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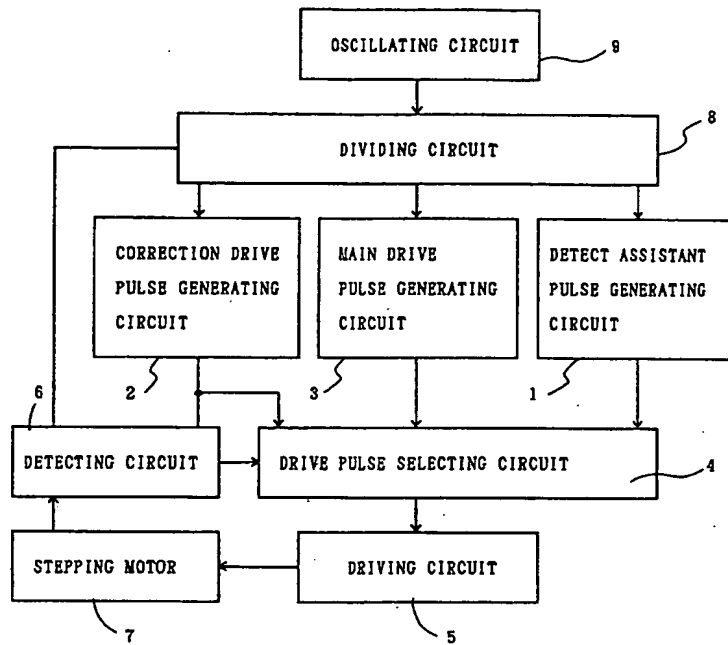
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54 **ELECTRONIC TIMEPIECE.**

57 This invention is directed to obtain a compact, low-power electronic timepiece which supplies a stepper motor with effective power depending on changes such as an increase of load of a step motor with time and variations of quality of components to improve accuracy of detection of revolution of a rotor. To amplify the voltage induced by rotation of the rotor that occurs after cut-off of a main driving pulse, a detection auxiliary pulse is supplied to the step motor so as to improve detection accuracy of revolution and to actuate the step motor with minimum necessary effective power.

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FIG. 1



Technical Field

This invention relates to an electronic timepiece in which plural detect assistant pulses are output to a stepping motor after turning off a main drive pulse, thereby performing stable detection of the rotation of the stepping motor.

Background Art

For a stepping motor for a recent electronic timepiece, a stepping motor driving means has been practically used in which a main drive pulse having low effective power is output to the stepping motor to reduce current-consumption, and then the rotational state of a rotor is detected by any means to output a correction drive pulse to the stepping motor in accordance with the detection result. Practical examples are disclosed in Japanese publication of applications No. 61-8392 and No. 63-18148, for example.

With respect to the practical example which has been known in Japanese publication of application No. 61-8392, Fig. 2 diagrammatically shows a drive voltage waveform of a correction drive system, and Fig. 3 diagrammatically shows a voltage waveform after turning off a main drive pulse obtained by the drive system as shown in Fig. 2.

The drive voltage waveform diagram as shown in Fig. 2 is constructed by a main drive pulse P1 (hereinafter referred to as "P1") which is output to the stepping motor every one second, a section DT for detecting the rotation of the stepping motor after the turning off P1, and a correction drive pulse P2 (hereinafter referred to as "P2") which is output when the stepping motor is in non-rotational state at P1. P1 automatically alters its pulse width in accordance with a load state to be applied to the stepping motor. P2 is output when the rotor cannot carry out its normal stepping operation at P1, and thus it is designed to have a pulse width of large effective power and output sufficient torque.

Fig. 3 shows a voltage waveform which is induced in a detection resistor by forming a closed loop in a coil after pulse turning off through the control of a MOS gate for driving the stepping motor or the like. As shown in Fig. 3, as a rotation detecting means for the rotor is used an identification method of electrically detecting whether this induced voltage reaches a predetermined voltage on the basis of the fact that the induced voltage in the section DT is different between a rotational state (as indicated by a solid line in Fig. 3) and a non-rotational state (as indicated by a dotted line in Fig. 3).

This detection means is characterized in that the rotor which is rotated with the main drive pulse makes a rotation free attenuating motion due to magnetic potential energy the rotor contains after the turning off the main drive pulse, and the variation of the induced voltage occurring in the coil during the attenuating motion is used as the rotation detecting means.

With respect to the practical example which is known in Japanese publication of application No. 63-18148, Fig. 4 shows an example of a drive voltage waveform diagram of a correction drive system, and Fig. 5 shows an example of a current waveform generated when the rotor is driven by the detection pulse.

The driving voltage waveform diagram of Fig. 4 is constructed by a main drive pulse P1 which is output to the stepping motor every one second, detection pulses Px and Py which are used to detect the rotation of the stepping motor after the turning off P1, and a correction drive pulse P2 which is output when the stepping motor is in a non-rotational state at P1. P1 and P2 are identical to those of Fig. 2. The detection pulses Px, Py have such a short pulse width that the stepping motor cannot be rotated.

Fig. 5 shows the current waveform when the rotor is driven with the detection pulse, and the current waveform is varied as shown by a line a or line b of Fig. 5 in accordance with the orientation of the magnetic pole of the rotor. The reason for the difference in current waveform is that the current waveform is determined in accordance with whether the magnetic pole formed in a stator with detection pulse is in a state where the magnetic pole of the rotor magnet has a repulsive orientation or an attractive orientation. As shown by a curved line of Fig. 5, the rotation detecting means for the rotor drives the rotor with the detection pulse, and identifies the orientation of the magnetic pole of the rotor on the basis of the difference in shape of the current waveform flowing in the coil at the driving time of the rotor, thereby to detect the rotation of the rotor.

The detecting means is characterized in that the rise-up voltage of the current waveform (the rise-up shape of the voltage waveform) is detected using the detection pulse having such effective power as to reduce the current consumption to detect the position of the magnetic pole of the rotor magnet, whereby the rotation of the rotor is detected.

However, the conventional rotation detecting method has the following problem for accurate judgment of the rotation of the rotor.

An induced voltage which is caused by a rotation free attenuating motion of the rotor within a predetermined time (for example, a period from the start of pulse application to 8 - 16 msec) has the relationship between the induced voltage and the pulse width of the main drive pulse as shown in Fig. 6 and the relationship between the induced voltage and the moment of inertia of the rotor as shown in Fig. 6.

5 The relationship between the main drive pulse and the pulse width is explained with the solid of Fig. 6 showing the induced voltage waveform.

When the main drive pulse is applied to the stepping motor, the induced voltage is kept to be sufficiently high voltage in a range of the shortest pulse width T1 to a degree of long pulse width T2 where a normal stepping operation can be performed. However, when the pulse width exceeds T2, the induced
10 voltage is rapidly lowered. This phenomenon is caused for the following reason: the rotor has low magnetic potential energy after a pulse having a long pulse width is turned off, and the amplitude of the attenuating motion of the rotor is reduced, so that the induced voltage is lowered in proportion to the amplitude of the attenuating motion of the rotor.

The relationship between the induced voltage and the inertia moment of the rotor is explained with the
15 solid of Fig. 6 showing the induced voltage waveform. A stepping motor having a rotor of low inertia moment can not only reduce power consumption but also easily rotate and stop. That is, the rotor of low inertia moment can be rotated with a small amount of effective power, and stopped in a short time after turning off a pulse through an attenuating motion of small amplitude. When the amplitude is small as described above, the absolute number of magnetic flux which intersects to the coil is small, and the induced
20 voltage caused by the attenuating motion of the rotor is also lowered. Further, since the rotation attenuating motion of the rotor is rapidly reduced, if a method of detecting the induced voltage in a predetermined time is used, the rotor almost approaches to a stopped state. Accordingly, there exists a little no induced voltage which is caused by variation of magnetic flux per unit time, and the rotation state of the rotor is erroneously judged to be a non-rotational state.

25 Accordingly, in the rotation detection method of the rotor using the induced voltage occurring after the application of the main drive pulse, if the power consumption is increased in order to lengthen the pulse width of the main drive pulse to improve a driving torque and the inertia moment of the rotor is reduced to lower the power consumption, the amplitude of the rotation free attenuating motion of the rotor after the turning off the pulse is lowered to induce the lowering of the induced voltage, resulting in the erroneous
30 judgment of the rotation of the rotor.

Further, in the detection method using the detection pulse, the pulse width of the detection pulse must be designed to be long to some extent to enable accurate judgment of the magnetic pole of the rotor, and thus there occurs a problem that the current consumption of the stepping motor is increased.

35 Still further, the judgment on the rotation of the rotor is erroneously made if the detection pulse is output from a rest state of the rotor, and thus the output timing of the detection pulse must be delayed. Accordingly, the output timing of the correction drive pulse which is output in the non-rotational state of the rotor is delayed, so that the motion of an indicator is delayed and then looked unnaturally.

40 An object of this invention is to solve the problem of the prior art, and to provide a compact electronic time piece which can improve precision of detection of the rotation of a rotor, and realize the low power consumption.

Disclosure of Invention

In order to solve the above problem, an electronic time piece having a stepping motor and a gear train
45 has a circuit construction comprising a detect assistant pulse generating circuit 1 for generating at least one detect assistant pulse which is such an effective power pulse that the stepping motor 7 is not rotated by one step, on the basis of a clock pulse input from a dividing circuit 8, and outputting the generated pulse to a drive pulse selecting circuit 4, a main drive pulse generating circuit 3 for generating at least one kind of main drive pulse signal on the basis of the clock signal input from the dividing circuit 8 and outputting the
50 generated pulse signal to the drive pulse selecting circuit 4, a correction drive pulse generating circuit 2 for generating a correction drive pulse signal longer than the main drive pulse on the basis of the clock signal input from the dividing circuit 8 and outputting the generated correction drive pulse signal to the drive pulse selecting circuit 4, the drive pulse selecting circuit 4 for selecting the output or non-output of the correction drive pulse signal in accordance with the main drive pulse signal, the detect assistant pulse signal and a
55 detection signal from a detecting circuit 6 and outputting the main drive pulse signal, the detect assistant pulse signal and the correction drive pulse signal to a driving circuit 5, said driving circuit 5 for converting the main drive pulse signal, the detect assistant pulse signal and the correction drive pulse signal input from the drive pulse selecting circuit 4 to effective power pulses and outputting the effective power pulses to the

stepping motor 7, and the detection circuit for carrying out a circuit switching operation on the basis of the clock signal input from the dividing circuit 8 to detect the rotation of said stepping motor 7 and generating a detection signal in accordance with a rotation detection result to output the detection signal to said detecting circuit 6, and the rotation of the stepping motor 7 can be accurately performed by applying the detect assistant pulse to the stepping motor 7, thereby to improve the detection precision.

In the electronic clock thus constructed, the detect assistant pulse is applied to the stepping motor after a predetermined time elapses after the interruption of the main drive pulse which is applied to the stepping motor every one second. The rotational angular velocity of the rotor which makes the rotation free attenuating motion after the interruption of the main drive pulse is amplified by the detect assistant pulse, and it is faster than before the application of the detect assistant pulse. The potential of the induced voltage occurring in the coil is heightened in proportion to the rotational angular velocity of the rotor.

It will be described with reference to Figs. 7(a) to (e) and Fig. 8 that by applying the detect assistant pulse as described above, the rotational speed of the rotor is increased and the amplitude of the rotation attenuating motion is intensified.

Fig. 7(a) is a schematic diagram showing that the rotor 70 is electrically stably at rest at an angle α . A magnetic potential energy difference occurs between notches 72, 73 provided to a stator 71 and magnet of the rotor 70, and the rotor rests at the angle at which the energy difference is lowest.

When the main drive pulse P1 as shown in Fig. 8 is applied in the rest state of the rotor as shown in Fig. 7(a), magnetic flux 75 occurs in a coil 74, so that magnetic pole occurs in the stator 71 as shown in Fig. 7(b), and the rotor 70 starts its rotation in a direction as indicated by an arrow using a magnetic repulsive force.

When the main drive pulse P1 is interrupted after the rotor magnetic pole N exceeds an angle β as shown in Fig. 8, the rotor 70 starts the rotation free attenuating motion so that it is at rest at an angle α 1 which provides a magnetically stable state. At this time, the rotor 70 occupies the magnetic potential energy and the rotational energy due to the inertia force by the main drive pulse.

Upon input of a detect assistant pulse Pa as shown in Fig. 8 to the driving circuit 5 when the rotor magnetic pole N reaches an angle γ as shown in Fig. 7(c), magnetic flux occurs in the coil, and the magnetic pole as shown in Fig. 7(c) is induced in the stator 71. The rotor 70 is supplied with rotational energy due to the magnetic repulse again, and the amplitude of the rotation free attenuating motion is intensified as shown by the waveform of the solid line of Fig. 8.

When the amplitude of the rotation free attenuating motion of the rotor is intensified, as shown in Fig. 7(d), the variation of the magnetic flux 75 which intersects to the coil 74 is also increased, and current induced in the coil 74 is increased. The waveform of the dotted line of Fig. 8 indicates a rotational state of the rotor when no detect assistant pulse is applied to the stepping motor, and the induced current is small because the amplitude of the rotor is low and the variation of the magnetic flux 75 intersecting to the coil 74 is small.

The rotor 70 after the interruption of the detect assistant pulse makes the rotation free attenuating motion as shown by the waveform of the solid line of Fig. 8, and then it stops at the magnetically stable angle as shown in Fig. 7(e).

As described above, the application of the detect assistant pulse Pa inducing the rotational motion of the rotor during the rotation free attenuating motion after the main drive pulse P1 intensifies the amplitude of the attenuating motion and the variation of the magnetic flux intersecting to the coil which is required to detect the rotation of the rotor, and thus it has an effect of increasing the induced voltage. Accordingly, according to this invention using the detection system of electrically comparing the induced voltage with a predetermined reference voltage, the potential of the induced voltage is heightened with the detect assistant pulse, and this enables the rotation detection of the stepping motor to be easily and accurately performed.

Brief Description of Drawings

Fig. 1 is a block diagram showing a first embodiment according to this invention.

Fig. 2 is a drive voltage waveform diagram showing an example of the conventional correction drive system.

Fig. 3 is a diagram showing an example of the voltage waveform due to the rotation free attenuating motion of the stepping motor after the interruption of the main drive pulse.

Fig. 4 is a drive voltage waveform diagram showing another example of the conventional correction drive system.

Fig. 5 is a diagram showing an example of the drive current waveform during the driving of the detect pulse.

Fig. 6 is an explanatory diagram showing the relationship between the pulse width and the induced voltage.

Fig. 7 (a) to (e) are diagrams showing the operation principle of the rotor of the embodiment of this invention.

5 Fig. 8 is a diagram showing the relationship between the drive pulse and the rotational angle of the rotor in the embodiment according to this invention.

Fig. 9 is a diagram showing the drive voltage waveform of the first embodiment according to this invention.

10 Fig. 10 is a circuit diagram showing an example of a main drive pulse generating circuit 3 in this invention.

Fig. 11 is a circuit diagram showing an example of a correction drive pulse generating circuit 2 in this invention.

Fig. 12 is a circuit diagram showing an example of a detect assistant pulse generating circuit 1 in this invention.

15 Fig. 13 is a circuit diagram showing an example of a drive pulse selecting circuit 4 in this invention.

Fig. 14 is a timing chart for input and output signals of the drive pulse selecting circuit 4 in this invention.

Fig. 15 is a circuit diagram showing an example of a driving circuit 5 in this invention.

Fig. 16 is a diagram showing paths of current flowing in a coil in the embodiment of this invention.

20 Fig. 17 is a circuit diagram showing an example of the detect circuit 6 of this invention.

Fig. 18 is a timing chart for an electrical operation of the drive circuit 5 and the detection circuit 6 of this invention.

Fig. 19 is a flowchart for the circuit operation of the first embodiment of this invention.

Fig. 20 is a block diagram of a second embodiment of this invention.

25 Fig. 21 is a diagram showing the drive voltage waveform of the second embodiment of this invention.

Fig. 22 is a circuit diagram showing an example of the detect assistant pulse output selecting circuit 10 of the second embodiment according to this invention.

Fig. 23 is a timing chart showing the electrical operation of the detect assistant pulse output selecting circuit 10 of the second embodiment according to this invention.

30 Fig. 24 is a flowchart showing the circuit operation of the second embodiment according to this invention.

Fig. 25 is a block diagram showing the third embodiment according to this invention.

Fig. 26 is a diagram showing the drive voltage waveform of the third embodiment according to this invention.

35 Fig. 27 is a circuit diagram showing an example of the detect assistant pulse with altering circuit 11 as shown in the third embodiment according to this invention.

Fig. 28 is a timing chart for the electrical operation of the detect assistant pulse width altering circuit 11 of the third embodiment according to this invention.

Fig. 29 is a flowchart showing the circuit operation of the third embodiment according to this invention.

40 Fig. 30 is a block diagram showing the fourth embodiment according to this invention.

Fig. 31 is a circuit diagram showing an example of the detect assistant pulse output counter circuit 12 of the fourth embodiment according to this invention.

Fig. 32 is a timing chart for the electrical operation of the detect assistant pulse output counter circuit 12 and the detect assistant pulse output selecting circuit 10.

45 Fig. 33 is a flowchart for the circuit operation of the fourth embodiment according to this invention.

Fig. 34 is a block diagram showing the fifth embodiment according to this invention.

Fig. 35 is a diagram showing the drive voltage waveform of the fifth embodiment according to this invention.

50 Fig. 36 is a circuit diagram showing an example of the detect assistant pulse output timing generating circuit 13 of the fifth embodiment according to this invention.

Fig. 37 is a timing chart for the electrical operation of the detect assistant pulse output timing generating circuit 13 of the fifth embodiment according to this invention.

Fig. 38 is a flowchart for the circuit operation of the fifth embodiment according to this invention.

Fig. 39 is a block diagram showing the sixth embodiment according to this invention.

55 Fig. 40 is a diagram showing the drive voltage waveform of the sixth embodiment according to this invention.

Fig. 41 is a circuit diagram showing an example of the detect assistant pulse output selecting circuit 10 of the sixth embodiment according to this invention.

Fig. 42 is a timing chart for the electrical operation of the detect assistant pulse output selecting circuit 10 of the sixth embodiment according to this invention.

Fig. 43 is a circuit diagram showing an example of the main drive pulse generating circuit of the sixth embodiment according to this invention.

5 Fig. 44 is a circuit diagram showing an example of the main drive pulse generating circuit of the sixth embodiment according to this invention.

Fig. 45 is a timing chart for the electrical operation of the main drive pulse generating circuit of the sixth embodiment according to this invention.

Fig. 46 is a flowchart for the circuit diagram of the sixth embodiment according to this invention.

10 Fig. 47 is a block diagram showing the seventh embodiment according to this invention.

Fig. 48 is a diagram showing the drive voltage waveform of the seventh embodiment according to this invention.

Fig. 49 is a circuit diagram showing an example of the detect assistant pulse width altering circuit 11 of the seventh embodiment according to this invention.

15 Fig. 50 is a timing chart for the electrical operation of the detect assistant pulse width altering circuit 11 of the seventh embodiment according to this invention.

Fig. 51 is a flowchart for the circuit operation of the seventh embodiment according to this invention.

Fig. 52 is a block diagram showing the eighth embodiment according to this invention.

20 Fig. 53 is a diagram showing the drive voltage waveform of the eighth embodiment according to this invention.

Fig. 54 is a circuit diagram showing an example of the detect assistant pulse output timing generating circuit 13 of the eighth embodiment according to this invention.

Fig. 55 is a timing chart for the electrical operation of the detect assistant pulse output timing generating circuit 13 of the eighth embodiment according to this invention.

25 Fig. 56 is a flowchart for the circuit operation of the eighth embodiment according to this invention.

Fig. 57 (a) to (d) show the drive voltage waveform showing a construction example of an alternating pulse in the ninth embodiment according to this invention.

Best Mode for Carrying Out the Invention

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(1) First Embodiment

The first embodiment is characterized in that a detect assistant pulse Pa is applied to a stepping motor which is subjected to a rotation detecting operation (see Fig. 9). The first embodiment of this invention will be described hereunder with reference to the drawings.

35 Fig. 1 is a block diagram of the first embodiment of this invention. An oscillating circuit (OSC) 9 usually includes a quartz oscillator, and oscillates a signal of 32768Hz. This signal is output to the dividing circuit 8. This signal is divided into clock signals having frequencies of 1Hz at minimum by 15-stage flip flops in the dividing circuit 8, and these clock signals of respective frequencies are output to the main drive pulse generating circuit 3, the correction drive pulse generating circuit 2, the detect assistant pulse generating circuit 1, and the detecting circuit 6.

40 Since the stepping motor 7 is supplied with a main drive pulse P1 which is an effective power pulse every one second, the main drive pulse generating circuit 3 generates a main drive pulse signal on the basis of the clock signal input from the dividing circuit 8, and outputs the main drive pulse signal to the drive pulse selecting circuit 4.

45 Since the stepping motor is supplied with a correction drive pulse 7 so that it can be surely rotated and complete a normal stepping operation, the correction drive pulse generating circuit 2 generates a correction drive pulse signal on the basis of the clock signal input from the dividing circuit 8, and outputs the correction drive pulse signal to the drive pulse selecting circuit 4 at a predetermined timing.

50 The detect assistant pulse generating circuit 1 generates a detect assistant pulse signal having such a pulse width that the stepping motor is not rotated on the basis of the clock signal input from the dividing circuit 8, and outputs the detect assistant pulse signal to the drive pulse selecting circuit 4 at a predetermined timing.

55 At arbitrary timing, the drive pulse selecting circuit 4 outputs to the driving circuit 5 a correction drive pulse signal for selecting the output or non-output in accordance with the detect signal output from the main drive pulse signal, the detect assistant pulse signal and the detection signal output from the detecting circuit. The correction drive pulse signal is output to the driving circuit 5 only when the rotation detection result of the rotor 70 judges the non-rotational state in the detecting circuit 6.

The driving circuit 5 supplies the main drive pulse signal, the detect assistant pulse signal and the correction drive pulse signal input from the drive pulse selecting circuit 4 to the stepping motor 7 as an effective power pulse.

The detecting circuit 6 generates a detect-section signal for carrying out detection of the rotation of the rotor at only a predetermined time on the basis of the signal input from the dividing circuit 8, executes the rotation detection operation of the stepping motor 7 in accordance with the signal, and outputs information on the rotation or non-rotation to the drive pulse selecting circuit 4 as a detection signal.

The output of the stepping motor 7, that is, the rotational motion is transferred to the ring array, the indicator, etc.

Next, an embodiment of each circuit as shown in the circuit block of Fig. 1 will be described.

First, the drive pulse generating circuit 3 will be described with reference to Fig. 10. The main drive pulse generating circuit 3 comprises a latch circuit 301 and a NOR gate 302, and generates a main drive pulse signal S302 every one second in synchronism with the rise-up signals of the clock signals 1Q and 64M input from the dividing circuit 8.

An embodiment of the correction drive pulse generating circuit 2 is designed shown in Fig. 11, and it comprises a latch circuit, a NOR gate, a NOT gate, an AND gate, etc. Through the operation of the correction drive pulse generating circuit 2, a correction drive pulse signal S202 as shown in a timing chart of Fig. 14 is output after 31.25msec elapses from the rise-up of 1Q. In this embodiment, the pulse comprises a combination pulse of a continuous pulse and an intermittent pulse to maximize the effect of the correction drive pulse P2.

An embodiment of the detect assistant pulse generating circuit 1 is designed as shown in Fig. 12, and it comprises latch circuits 102, 103, NOR gates 101, 104, etc. The detect assistant pulse generating circuit 1 starts the output of a detect assistant pulse signal S101 after 4.9 msec elapses from the rise-up of 1Q, and interrupts the output of the detect assistant pulse signal in accordance with a clock signal 512Mbar to the latch circuit 103. The output timing of the detect assistant pulse signal S101 is shown in the timing chart of Fig. 14.

The drive pulse selecting circuit is designed as shown in Fig. 13, and comprises OR gates 401, 402, an AND gate 403, a flip-flop 404 (hereinafter referred to as TFF), a gate circuit 405, a NAND gate circuit 406, a NOT gate 407, etc. The OR gate 401 is provided to selectively output a pulse signal input to each pulse generating circuit. The input terminal thereof is supplied with the signals S101, S302 and S403. The OR gate 402 is provided to synthesize a pole inverting signal S402 which controls the pole of the voltage of an applied pulse and is supplied to the TFF 404. The input terminal thereof is supplied with the signals S101, S302 and S407. The AND gate 403 is provided to control the output or non-output of the correction drive pulse.

The drive pulse signal S401 which is an output signal of the OR gate 401 is input to the gate circuit 405. On the other hand, the pole inverting signal which is the output signal of the OR gate 402 is input to a T terminal of the TFF 404. In accordance with a trailing signal of the pole inverting signal S402, the output signals S404Q and S404QX of the TFF 404 are inverted to "High (hereinafter referred to as "H")" or "Low (hereinafter referred to as "L")". The TFF output signals S404Q and S404QX are input to the gate circuit 405 and the NAND gate 406.

The gate circuit 405 and the NAND gate circuit 406 outputs driving MOSFET control signals S405A to D for controlling ON/OFF of a stepping motor driving MOSFET to gate terminals of MOSFETs 501 to 504 as shown in Figs. 15(a), (b) in accordance with the drive pulse signal S404, the TFF output signals S404Q and S404QX and the MOSFET control signals S606 and S602 input from the detecting circuit 6. Further, detecting MOSFET control signals S406A, S406B for controlling the ON/OFF of the detecting MOSFET are output to the gate terminals of MOSFETs 505, 506 as shown in Figs. 15(a), (b).

An embodiment of the driving circuit 5 is designed as shown in Figs. 15(a), (b), and comprises motor driving MOSFETs 501 to 504, detecting MOSFETs 505, 506 and resistant elements 507, 508. The MOSFETs 501 to 506 carry out an ON/OFF operation in accordance with an input signal to the gate terminal of each MOSFET. The rotation of the stepping motor 7 is realized by applying drive pulses P511 and P512 to the stepping motor 7 from the output terminals 511, 512 which are connected to the coil 74.

Current paths in accordance with a switching operation of each MOSFET is shown in a table 1 and Figs. 14 and 16.

[Table 1]

	501	502	503	504	505	506	current path
5	on	off	on	off	off or on	off or	(4)
	on	off	off	on	off	off	(1)
	off	on	on	off	off	off	(2)
10	on	off	off	off	off	on	(3)
	off	off	on	off	on	off	(5)

Fig. 14 shows a timing chart for the control signals S405A to S405D and S406A, S406B of each MOSFET which is input to the driving circuit 5. Fig. 16 is a schematic diagram showing a path of current flowing in the coil.

The paths (1) and (2) are current paths for driving pulses through which currents flowing in opposite directions are applied to the coil. The paths (3),(5) are closed loops of high impedance containing detection resistor 507 or 508 (resistant element of several hundreds K . The path (4) is in a state where both ends of the coil 74 are short-circuited. When the MOSFET 505 or 506 is in ON-state, there are two paths through which current flows. However, only the path (4) is regarded as the current-flowing path due to the affection of the detection resistors. [0039]

An embodiment of the detecting circuit 6 is designed as shown in Fig. 17, and comprises an AND gate 601, a gate circuit 602, an OR gate 603, a comparator 605, a latch circuit 606, a reference voltage generating resistant element 604, etc. The detecting operation of the detecting circuit 6 is as follows.

First, the input signals S507, S508 and S604 to the comparator 605 will be described. The signal S604 is a reference voltage VTH (hereinafter referred to as VTH) for judgment on rotation, and is a potential induced by the resistant element 604. The signal S507, S508 is a detection voltage VRS (hereinafter referred to as VRS) obtained by amplifying the induced voltage occurring in the coil with the detection resistor 507, 508, and VRS is also a transient voltage which is caused by a switching operation over multiple period of the path (3) or (4) and the path (5) as shown in Fig. 16. The comparator is set to "L" for " $VTH \leq VRS$ ", and to "H" for " $VTH > VRS$ ". The comparator output signal S605 is output to a SET terminal of the latch circuit 606. The timing chart for the above detecting operation is shown in Fig. 18.

Fig. 18 shows motor drive pulses P511, P512 which are output from the driving circuit 5 to the stepping motor 7, rotation detection voltages S507, S508 which are input from the stepping motor 7 to the detecting circuit 6, a signal S605 which is obtained and output through electrical comparison between the VTH and the rotation detection voltage in the detecting circuit 6, and a detection signal S606 which is the output signal of the detecting circuit 6.

For first one second, the main drive pulse is applied to the stepping motor from the 511 terminal side of Fig. 18, and the detect assistant pulse is applied from the 512 terminal side. However, the rotor is in the non-rotational state, the comparator output signal S605 and the detection signal S606 are left in "L" state, the correction drive pulse is applied to the stepping motor.

For next one second, the main drive pulse is applied to the stepping motor from the 512 terminal side of Fig. 18, and the detect assistant pulse is applied to the 511 terminal side. Thereafter, the rotor is rotated, and thus the signal S605 becomes one shot "H" and the detection signal S606 also becomes "H". When the detection signal is "H", the correction drive pulse is not applied to the stepping motor, and thus the drive pulse P512 has no voltage waveform of the correction drive pulse.

When a master signal of 1Hz is "H", the latch circuit 606 is in a reset state, and the detection signal S606 is also "L".

Next, the operation of the embodiment according to this invention will be described with reference to a flowchart of Fig. 19.

First, simultaneously with the start (2001), initialization is made to the gate circuit, etc. (2002). Subsequently, the main drive pulse P1 is output to the stepping motor (2003), and then the detect assistant pulse Pa is output to the stepping motor after the main drive pulse is interrupted (2004). After interruption of the detect assistant pulse, the program goes to a subsequent rotation detecting operation.

At the rotation detecting step (2005), the rotation or non-rotation of the rotor is judged. The detection method uses comparison between VTH and VRS. If $|VRS| \leq |VTH|$, the correction drive pulse P2 is output to the stepping motor (2006). On the other hand, if $|VRS| > |VTH|$, no correction drive pulse is output, and the operation of rotating the rotor by one step is terminated.

The above description is made for the first embodiment. The circuit of this embodiment is characterized in that the detect assistant pulse is applied to the motor, and has an object of improving the precision of the rotation detection by applying the detect assistant pulse.

5 (2) Second Embodiment

The circuit construction of the second embodiment of this invention is characterized in that a detect assistant pulse output selecting circuit 10 is added to the circuit construction of the first embodiment as described above (see a block diagram of Fig. 20), and the output of the detect assistant pulse signal is selected in accordance with the detection signal input from the detecting circuit 6 (see Fig. 21).

10 An embodiment of the detect assistant pulse output selecting circuit 10 is designed as shown in Fig. 22, and comprises an RS latch circuit 1001, an OR gate 1002, AND gates 1003, 1005, and a NOR gate 1004. A timing chart for a series of operations of the detect assistant pulse output selecting circuit 10 is shown in Fig. 23.

15 Signals input to the detect assistant pulse output selecting circuit 10 are a detect assistant pulse signal S101, a detection signal S606 from the detection circuit 6, an output signal S202 from the correction drive pulse generating circuit and a reset signal.

The NOR gate 1004 is connected to the SET terminal of the RS latch circuit 1001. When the correction drive pulse signal S201 falls down to "L" with the signal S606 being left in "L" state, the output signal S1004 outputs "H" to the RS latch circuit 1001, and the RS latch circuit 1001 is set to a SET state (output "H" from the output terminal Q).

With respect to the AND gate 1003, when the rotor is rotated and the RS latch circuit 1001 is in the SET state, the output signal S1003 of the AND gate 1003 is set to "H", and input to the OR gate 1002.

20 The OR gate 1002 is connected to the RESET terminal of the RS latch circuit 1001. When the reset signal or signal S1003 rises up to "H", the RS latch circuit 1001 is set to the RESET state (outputs "L" from the output terminal Q).

The RS latch circuit 1001 is set to the SET state if the rotor is detected to be in the non-rotational state, and set to the RESET state if the rotation of the rotor is detected when the signal S1001 is in "H" state (SET state). Although the rotor is detected in the RESET state (the signal S1001 is "L"), the signal S1001 is not varied.

30 The AND gate 1005 outputs the detect assistant pulse signal S1005 to the OR gate 401 of the drive pulse selecting circuit 4 when the RS latch circuit 1001 is in the SET state.

Next, the operation of the circuit of this embodiment according to this invention will be described with reference to a flowchart of Fig. 24.

35 Simultaneously with the start (2001), the initialization is made to the circuit (2007) to set a control signal m1 to "m1=0". The main drive pulse P1 is output to the stepping motor (20039, and then it is determined using the control signal m1 whether the detect assistant pulse is output to the stepping motor (2008). If the control signal m1 is in a state of "m1=1", a next detect assistant pulse Pa is output after the interruption of the main drive pulse (2004). On the other hand, if the control signal m1 is in a state of "m1=0", the detect assistant pulse Pa is not output to the stepping motor.

40 Subsequently, after the interruption of the detect assistant pulse, the program goes to a next rotation detecting operation.

At the rotation detecting step (2005), the rotation or non-rotation of the rotor is judged. The detection method uses the comparison between VTH and VRS. If $|VRS| \leq |VTH|$, the correction drive pulse P2 is output to the stepping motor (2006). Thereafter, the judgment on the control signal m1 is made (2009). If "m1=0", the control signal m1 is written to "m1=1" (2011).

On the other hand, if $|VRS| > |VTH|$, the correction drive pulse P2 is not output to the stepping motor, and the control signal m1 is written to "m1=0" (2010). Subsequently, the operation of rotating the rotor by one step is terminated.

50 By repeating the above operation, the output or non-output of the detect assistant pulse can be controlled in accordance with the rotation detection result of the rotor, and the output of the detect assistant pulse which exceeds a required amount can be prevented. Therefore, the detection precision can be improved, and the power consumption can be suppressed.

55 (3) Third embodiment

The circuit construction of the third embodiment according to this invention is characterized in that a detection assistant pulse width altering circuit 11 is added to the circuit construction of the first embodiment

as described above (see a block diagram of Fig. 25), and the pulse width of the detect assistant pulse signal is alterable in accordance with the detection signal input from the detecting circuit 6 (see Fig. 26).

An embodiment of the detect assistant pulse output selecting circuit 11 according to this invention is designed as shown in Fig. 27. It selects one clock signal S1101 from plural clock signals input from the dividing circuit 8 in accordance with the detection signal S606 of the detecting circuit 6, and outputs the selected signal to the detect assistant pulse generating circuit 1. The timing chart for the output timings of these signals is shown in Fig. 28.

The circuit construction of an embodiment of the detect assistant pulse width altering circuit 11 of the third embodiment of this invention and the operation thereof will be first described.

The detect assistant pulse width altering circuit 11 comprises a NAND gate 1101, a gate circuit 1102, a latch circuit 1103, a gate circuit 1104, an OR gate 1105, etc.

The input signals of the gate circuit 1104 are S201 and S606. The gate circuit 1104 synthesizes output signals S1104a, S1104b which are rise-up signals synchronized with S201 in accordance with the rotation or non-rotation of the rotor, and outputs the output signals S1104a and S1104b to the SET terminal of the latch circuit 1103 and the input terminal of the OR gate 1105, respectively.

The input signals of the OR gate 1105 are S1104 and RESET signal as described above, and the output terminal is connected to the RRESET terminal of the latch circuit 1103.

The latch circuit 1103 sets the output signal S1103a at the output terminal Q to "H" in a SET state (an electrical state after the input signal S1104a is set to "H"), and sets the output signal S1103b at the output terminal QX to "H" in a RESET state (an electrical state after the input signal S1105 is set to "H").

The input signals of the gate circuit 1102 are the signals S1103a and S1103b, a signal (2KMbar signal) obtained by inverting the master signal of 2KHz, and the master signal of 1KHz. When the input signal S1103 is "H", the output signal S1102a becomes a trailing clock signal synchronized with the 2KMbar signal (the signal S1102b is left in "H"-state). When the input signal S1103b is "H", the output signal S1102b is a clock signal synchronized with the 1KM signal (the signal S1102a is left in "H"-state).

The NAND gate 1101 is a gate element for outputting the input signals S1102a, S1102b as one clock signal, and the output signal S1101 thereof becomes a rise-up clock signal for any one of the 2KMbar signal and the 1KM signal. The output terminal is connected to the gate terminal of the latch circuit 103.

The relationship between the pulse width of the detect assistant pulse signal S101 and the clock signal S1101 is as shown in a table 2.

[Table 2]

Detection result of previous stepping operation	Signal S1101	Pulse width of S101
Rotation	2KMbar	0.122(msec)
non-rotation	1KM	0.244(msec)

With respect to the selection of the clock signal in the detect assistant pulse width altering circuit 11 of the third embodiment, selection of two kinds of clock signals is made. If the detecting circuit judges "rotation", the circuit is set to the SET state. If it judges "non-rotation", the circuit is set to the RESET state. If plural clock signals are required to be selected by the detect assistant pulse width altering circuit 11, the input signal may be controlled using a counter or the like.

Next, the operation of the circuit of the third embodiment according to this invention will be described with reference to a flowchart of Fig. 29.

First, simultaneously with the start (2001), the initialization is made to the circuit (2012) to set a control signal m2 (signal S1103a as shown in Fig. 27, for example) to m2=0. After the main drive pulse P1 is output to the stepping motor (2003), the pulse width of a next detect assistant pulse Pa is selected (2013). The output selection to the detect assistant pulse Pa is made using the control signal m2. If m2 = 0, the detect assistant pulse Pa is set to Pa=Pa0 (for example, Pa0=0.122msec) (2014), and output to the stepping motor (2016). On the other hand, if m2=1, the detect assistant pulse Pa is set to Pa=Pa1 (for example, Pa1=0.244 msec) (2015), and output to the stepping motor (2016).

Further, after the interruption of the detect assistant pulse, the program goes to a next rotation detecting operation.

At the rotation detecting step (2005), the rotation or non-rotation of the rotor is judged. The detection method uses the comparison between VTH and VRS. if $|VRS| \leq |VTH|$, the correction drive pulse P2 is output to the stepping motor (2006). Thereafter, the control signal m2 is rewritten to the signal of "m2=1"

(2017).

On the other hand, if $|VRS| > |VTH|$, the correction drive pulse P2 is not output to the stepping motor, and the control signal m2 is rewritten to "m2=0" (2018). Subsequently, the operation of rotating the rotor by one step is terminated.

5 By repeating the above operation, the control for the alteration of the pulse width of the detect assistant pulse can be performed in accordance with the rotation detection result of the rotor. The precision of the rotation detection can be improved by executing the pulse width altering operation of the detect assistant pulse. Pa0, Pa1 can be easily determined on an electrical circuit, and it is not necessary to specify the pulse width as described above.

10

(4) Fourth Embodiment

The circuit construction of the fourth embodiment according to this invention is characterized in that a detect assistant pulse output counter 12 is added to the circuit construction of the second embodiment as described above (see a block diagram of Fig. 30), and that the output frequency of the detect assistant pulse signal is counted, and in accordance with the detection signal input from the detecting circuit 6 and the count result, the output or non-output of the detect assistant pulse signal is selected.

15 An embodiment of the detect assistant pulse output selecting circuit 10 and the detect assistant output counter 12 of this embodiment according to this invention is a circuit as shown in Fig. 31. Fig. 32 shows a timing chart for the circuit. The circuit construction of the fourth embodiment of this invention and the operation thereof will be described with reference to Figs. 31 and 32.

The detect assistant pulse output counter 12 comprises a NOR gate 1201, a NAND gate 1202, a counter 1203 and an OR gate 1204.

25 The counter 1203 is a 2-bit binary counter, and switches the output signals S1203a, S1203b of the counter 1203 to "H" or "L" in synchronism with the trailing of the signal S1005 to output four kinds of combination signals (for example, S1203a is "H", and S1203b is "L" to the NAND gate 1202.

The NAND gate 1202 sets the signal S1202 to "L" only when the signals S1203a and S1203b are "H". The signals S1203a and S1203b are set to "H" only when a signal is input to the counter 1203 after reset at three times.

30 The NOR gate 1201 is synchronized with the master signal of 1Hz. When all the input signals are "L", the output signal S1201 is set to "H".

The OR gate 1204 is supplied with the RESET signal and the signal S1004, and the output signal S1204 thereof is output to the reset terminal of the counter 1203.

35 The detect assistant pulse output selecting circuit 10 comprises a latch circuit 1001, AND gates 1003, 1005, an OR gate 1002 and a NOR gate 1004.

The latch circuit 1001 inverts the data of the output signal S1001 in synchronism with the rise-up of the input signal. Accordingly, the output signal S1001 is set to "H" when the input signal S1004 to the SET terminal rises up, and the output signal S1001 is set to "L" when the input signal S1002 to the RESET terminal rises up.

40 The output terminal of the AND gate 1005 is connected to the OR gate 401 of the drive pulse output selecting circuit 4 and the T terminal of the TFF 1203 of the detect assistant pulse output counter 12. The input signals to the AND gate 1005 are the detect assistant pulse signal S101 and the signal S1001, and the AND gate 1005 outputs the input signal S101 as an output signal S1005 thereof only when the signal S1001 is "H".

45 The input signals to the AND gate 1003 are the detection signal S606 from the detecting circuit 6, the output signal S1201 of the detect assistant pulse output counter 12, and the signal S1001. The output terminal thereof is connected to the OR gate 1002, and the signal S1003 is set to "H" when all the input signals are "H".

50 The output terminal of the OR gate 1002 is connected to the RESET terminal of the latch circuit. The input signals thereto are the RESET signal and the signal S1003, and the signal S1002 is set to "H" when any one of those signals is set to "H".

The output terminal of the NOR gate 1004 is connected to the SET terminal of the latch circuit and the OR gate 1204. The input signals thereto are the inverted signal of the signal S606 and the signal S201. The output signal S1002 thereof is set to "L" when the rotor is rotated, and set to "H" when the rotor is not rotated.

55 The above description is made for the circuit construction of the fourth embodiment according to this invention and the operation thereof.

The operation of the circuit of the fourth embodiment according to this invention will be next described with reference to a flowchart of Fig. 33.

First, simultaneously with the start (2001), the initialization of the circuit (2019) is made to set a counter variable M to $M=0$ and set the control signal $m1$ (signal S1001 as shown in Fig. 31) to $m1=0$. Subsequently, the main drive pulse $P1$ is output to the stepping motor (2003), and then it is judged using the control signal $m1$ whether a next detect assistant pulse is output to the stepping motor (2008). If " $m1=1$ ", the next detect assistant pulse Pa is output to the stepping motor after the interruption of the main drive pulse (2004). On the other hand, if " $m1=0$ ", the detect assistant pulse Pa is not output to the stepping motor.

Further, after the interruption of the detect assistant pulse, the process goes to the next rotation detecting operation.

At the rotation detecting step (2005), the rotation or non-rotation of the rotor is judged. The detecting method uses the comparison between VTH and VRS . If $|VRS| \leq |VTH|$, the correction drive pulse $P2$ is output to the stepping motor (2006). Thereafter, the control signal $m1$ is identified (2020). If " $m1=1$ ", the counter variable is rewritten to " $M=0$ " (2021). If " $m1=0$ ", the counter variable M and the control signal $m1$ are rewritten to " $M=0$ " and " $m=1$ ", respectively (2022).

On the other hand, at the rotation detecting step (2005), if $|VRS| > |VTH|$, the control signal $m1$ is first identified (2023). If " $m1=1$ ", the count value of the counter variable M is identified (2024). If " $M=3$ ", the data of the control signal $m1$ and the counter variable M are reset to " $m1=0$ " and " $M=0$ ", respectively (2025). If " M is not equal to 3", the counter variable M is incremented as follows: " $M=M+1$ " (2026). If " $m1$ is not equal to 1", no data rewriting operation is carried out on the control signal $m1$ and the counter variable M . Subsequently, the operation of rotating the rotor is terminated.

By repeating the above operation, the output or non-output of the detect assistant pulse can be controlled in accordance with the rotation detection result of the rotor. If the detect assistant pulse is output once in consideration of a load torque by a calender by which a load is applied to the stepping motor for a long time, the output of the detect assistant pulse is continued during several stepping operation period, so that the precision of the rotation detection is improved.

(5) Fifth Embodiment

The circuit construction of the fifth embodiment according to this invention is characterized in that a detect assistant pulse output timing generating circuit 13 is added to the circuit construction of the first embodiment as described above (see a block diagram of Fig. 34), the timing of starting the output of the detect assistant pulse signal is altered (varied) in accordance with the detection signal input from the detecting circuit 6 (see Fig. 35).

An embodiment of the detect assistant pulse output timing generating circuit 13 of this embodiment according to this invention is a circuit as shown in Fig. 36, and Fig. 37 shows a timing chart. The circuit construction of an embodiment in the fifth embodiment of this invention and the operation thereof will be described with reference to Figs. 36 and 37.

The detect assistant pulse output timing generating circuit 13 comprises OR gates 1301, 1305, 1306, an NOR gate circuit 1302, an RS latch circuit 1303 and a gate circuit 1304.

The gate circuit 1304 outputs a signal S1304a to the SET terminal of a latch circuit 1303 in accordance with two kinds of signals of the detection signal S606 from the detecting circuit 6 and the output signal S201 from the correction drive pulse, and outputs a signal S1304b to the OR gate 1305. When the detection signal is "L (non-rotation)", S1304a is set to "H", and when the detection signal is "H (rotation)", S1304b is set to "H".

The OR gate 1305 outputs "H" signal to the RESET terminal of the latch circuit 1303 when any one of the RESET signal and the signal S1304b is set to "H".

The latch circuit 1303 sets the signal S1303a to "L" in the RESET state, and sets the signal S1303b to "L" in the SET state.

The NOR gate circuit 1302 is input with a signal S1306 which is synthesized in the OR gate 1306 from inverted master signals (64Mbar and 256Mbar) from the dividing circuit 8, a master signal of 1024Mbar, and the signals S1303a and S1303b. The NOR gate circuit 1302 outputs "H" at a combination timing at which the input signals are "L". There are two output signals, and these output signals S1302a and S1302b are input to the OR gate 1301. The output signal S1302a rises up after 4.88 msec elapses from the rise-up of the IQ signal, and the output signal S1302b rises up after 5.13 msec elapses from the trailing of the IQ signal.

The OR gate 1301 is provided to set both of the two output signals S1302a and S1302b to one detect assistant pulse output timing altering signal S1301.

The detect assistant pulse output timing altering circuit 13 as described above with reference to Fig. 36 is operated in accordance with the detection signal S606, whereby the output timing of the detect assistant pulse signal can be altered.

The operation of the circuit of the fifth embodiment of this invention will be next described with reference to a flowchart of Fig. 38.

First, simultaneously with the start (2001), the initialization is made to the circuit to set the control signal m3 (for example, the signal S1303a as shown in Fig. 36) to "m3=0". After the main drive pulse P1 is output to the stepping motor (2003), the output timing of a next detect assistant pulse Pa is selected (2028). The selection of the output timing of the detect assistant pulse Pa is carried out using the control signal m3. If "m3=0", the detect assistant pulse output timing ITPa is set to "ITPa=ITPa0 (for example, ITPa0=4.88 msec)" (2029), and output to the stepping motor (2031).

On the other hand, if "m3=1", the detect assistant pulse output timing ITPa is set to "ITPa=ITPa1 (for example, ITPa1=5.13 msec)" (2030), and output to the stepping motor (2031).

Further, the process goes to the next rotation detecting operation after the interruption of the detect assistant pulse.

At the rotation detecting step (2005), the rotation or non-rotation of the rotor is judged. The detection method uses the comparison between VTH and VRS. If $|VRS| \leq |VTH|$, the correction drive pulse P2 is output to the stepping motor (2006).

Thereafter, the control signal m3 is rewritten to the signal "m3=1" (2032).

On the other hand, if $|VRS| > |VTH|$, the correction pulse is output to the stepping motor, and the control signal m3 is rewritten to "m3=0" (2033). Thereafter, the operation of rotating the rotor by one step is terminated.

By repeating the above operation, the start time of the output timing of the detect assistant pulse can be altered in accordance with the rotation detection result of the rotor. By executing the altering operation of the output timing start time of the detect assistant pulse, the precision of the rotation detection can be improved.

(6) Sixth Embodiment

The circuit construction of the sixth embodiment of this invention is characterized in that a detect assistant pulse output selecting circuit 10 is added to the circuit construction of the first embodiment (see a block diagram as shown in Fig. 39), and the output or non-output of the detect assistant pulse signal is selected in accordance with the gate output signal of the main drive pulse generating circuit 3 (see Fig. 40).

The main drive pulse generating circuit 3 will be first described with reference to Figs. 43 and 44. The main drive pulse generating circuit 3 comprises an up-counter 303 comprising a TFF, a NAND gate, etc., a gate circuit 304 for dividing the output signals (S303 to S308) of the up-counter 303 to eight kinds of gate output signals (S309 to S316), a gate circuit 305 for synchronizing the gate output signals S309 to S316 of the gate circuit 304 with the master signal from the dividing circuit 8 and generating an interrupting timing signal S317 for the main drive pulse, a gate circuit 306 using a latch circuit for generating a main drive pulse signal S318 every one second, etc.

The input gate of the up-counter 303 is supplied with the output signal S606 of the detecting circuit 6 and the output signal S201 from the correction drive pulse generating circuit.

The timing chart as shown in Fig. 45 shows the input signal S319 and the output signals S303 to S308 of the up-counter 303, the gate output signals S309 to S316 of the gate circuit 304, and the main drive pulse signal S318. In order to clarify the operation of the main drive pulse generating circuit 3, Fig. 45 shows an operation in which the rotor is in the non-rotational state at all times.

An embodiment of the detect assistant pulse output selecting circuit 10 of this embodiment according to this invention is designed as shown in Fig. 41, and Fig. 42 shows the timing chart therefor. The circuit construction of an embodiment in the sixth embodiment of this invention and the operation thereof will be hereunder described with reference to Figs. 41 and 42.

The embodiment of the detect assistant pulse output selecting circuit 10 is designed as shown in Fig. 41, and comprises an AND gate 1006, an OR gate 1007, a NOR gate 1008, etc.

The OR gate 1007 outputs an "H" signal to the AND gate 1006 when any one of the gate output signals S315, S316 is "H".

The NOR gate 1008 outputs an "H" signal to the AND gate 1006 when all the gate output signals S309 to S314 are "L".

The AND gate 1006 outputs the detect assistant pulse signal S101 to the OR gate 401 as a signal S1006 when the input signals S1007, S1008 are "H".

Fig. 42 shows the timing chart for the circuit operation as described above, and shows the input signals S318 and S314 to S316 from the main drive pulse generating circuit 3, the detect assistant pulse signal S101, and the signals S401 and S403 of the drive pulse selecting circuit 4.

Only when the gate output signal S315 or S316 is "H", the detect assistant pulse signal S1006 is output to the OR gate 401 of the drive pulse selecting circuit 4. On the other hand, when any one of the main drive pulse selecting signals S309 to S314 is "L", the signal S1006 is left to be "L" irrespective of the rotation detection result, and the signal S1006 is not input to the OR gate 401.

The circuit operation of the sixth embodiment of this invention will be described with reference to a flowchart of Fig. 46.

First, simultaneously with the start (2001), the initial setting (2034) is made to set a counter variable n to " $n=0$ ". The main drive pulse P1 is set to $P1 = P0 + n\Delta P1$ (2035). At this time, P0 has the shortest pulse width (for example, $P0 = 1.95\text{msec}$), n is set to 0 to 7, and $\Delta P1$ is set to 0.244msec.

After the setting of the main drive pulse P1, the main drive pulse P1 is output to the motor (2036), and the output or non-output of the next detect assistant pulse Pa is judged (2037). The judgment on the output or non-output is carried out using the counter variable n . If " $n \geq 6$ ", the detect assistant pulse Pa is output (2004), and if " $n < 5$ ", the detect assistant pulse Pa is output to the motor.

In the next rotation detecting operation (2005), the rotation or non-rotation of the rotor is judged. The detection method uses the comparison between VTH and VRS. If $|VRS| \leq |VTH|$, the correction drive pulse P2 is output (2006), the counter variable n is incremented as follows: " $n = n + 1$ " (2038), and the operation of rotating the rotor is terminated.

The above description is for the operating flowchart. P0, $\Delta P1$, Pa0, ΔPa can be easily determined on the electrical circuit, and these values are not necessary to be limited to the above values.

(7) Seventh Embodiment

The circuit construction of the seventh embodiment is characterized in that a detect assistant pulse width altering circuit 11 is added to the circuit construction of the first embodiment as described above (see a block diagram as shown in Fig. 47), and the output or non-output of the detect assistant pulse signal is selected in accordance with the gate output signal of the main drive pulse generating circuit 3 (see Fig. 48).

An embodiment of the detect assistant pulse width altering circuit 11 of this embodiment according to this invention is designed as shown in Fig. 49, and Fig. 50 is a timing chart diagram. The circuit construction of an embodiment in the seventh embodiment according to this invention and the operation thereof will be described with reference to Figs. 49 and 50.

The detect assistant pulse width altering circuit 11 comprises an OR gate 1108, gate circuits 1106 and 1107, etc.

The gate circuit 1106 outputs a signal S1106a or S1106b to the OR gate 1108 when any one of the gate output signals S315 and S316 of the main drive pulse generating circuit 1 is "H".

The gate circuit 1107 outputs a master signal 2048 from the dividing circuit 8 to the OR gate 1108 as an output signal S1107 when any one of the gate output signals S309 to S314 of the main drive pulse generating circuit 1 is "H".

The OR gate 1108 outputs any one of input signals S1106a, S1106b and S1107 to the gate terminal of the latch circuit 103 in the detect assistant pulse generating circuit as an output signal S1108.

In accordance with the output signal S1108, the signal S103 in the detect assistant pulse generating circuit 1 is synthesized, and the timing for interrupting the detect assistant pulse signal S101 is controlled, whereby alteration of the pulse width of the detect assistant pulse signal S101 is realized.

Next, the operation of the circuit of this embodiment will be described with a flowchart of Fig. 51.

First, simultaneously with the start (2001), the initial setting (2034) is made to set the counter variable n to " $n=0$ ". The main drive pulse P1 is set to $P1 = P0 + n\Delta P1$ (2035). At this time, P0 have the shortest pulse width (for example, $P0 = 1.95\text{msec}$), n is set to 0 to 7, and $\Delta P1$ is set to 0.244 msec.

After the setting of the main drive pulse P1, the main drive pulse P1 is output to the motor (2036), and the pulse width of a next detect assistant pulse Pa is selected (2039). The counter variable n is used for the selection of the pulse width. If " $n < 5$ ", the pulse width of the detect assistant pulse Pa is set to " $Pa = Pa0$ " (2040), and the detect assistant pulse Pa is output (2042). On the other hand, if " $n \geq 5$ ", the pulse width of the detect assistant pulse Pa is set to " $Pa = Pa0 + (n-5)\Delta Pa$ " (2041), and the detect assistant pulse Pa is output (2042).

In the next rotation detecting operation (2005), the rotation or non-rotation of the rotor is judged. The detection method uses the comparison between VTH and VRS. If $|VRS| \leq |VTH|$, the correction drive pulse P2 is output (2006), and the counter variable n is incremented as follows: " $n = n + 1$ " (2038), thereafter terminating the operation of rotating the rotor.

- 5 The above description is for the operating flowchart. P0, P1, Pa0, Pa can be easily determined on the electrical circuit, and thus these values are not necessarily to be limited to the above pulse width.

(8) Eighth embodiment

- 10 The circuit construction of the eighth embodiment according to this invention is characterized in that a detect assistant pulse output timing generating circuit 13 is added to the circuit construction of the first embodiment as described above (see a block diagram as shown in Fig. 52), and the output start timing of the detect assistant pulse signal is altered in accordance with the gate output signal of the main drive pulse generating circuit 3 (see Fig. 53).

- 15 Fig. 54 shows an embodiment of the detect assistant pulse output timing generating circuit 13 of the embodiment according to this invention, and Fig. 55 is a timing chart diagram. The circuit construction of an embodiment in the eighth embodiment according to this invention and the operation thereof will be described with reference to Figs. 54 and 55.

- The detect assistant pulse output timing generating circuit 13 comprises OR gates 1307, 1311, a gate circuit 1308, a NOR gate 1309, a NOT gate 1310, etc.

The NOR gate 1309 sets an output signal S1309 to "L" when any one of the gate output signals S309 to S315 of the main drive pulse generating circuit is "H", outputs the signal to the gate circuit 1308.

The NOT gate 1310 inverts the gate output signal S316 of the drive pulse generating circuit, and outputs the signal S1310 to the gate circuit 1308.

- 25 The OR gate 1311 outputs to the gate circuit 1308 the composite signal S1311 of the inverted master signals 64Mbar and 256Mbar of the dividing circuit 8.

- The gate circuit 1308 is input with signals S1309, S1310 and S1311 and the inverted master signal 1024Mbar of the dividing circuit 8, and outputs the output signal S1308a based on the signal S1311 to the OR gate 1307 when the gate output signal S316 is "H". When any one of the gate output signals S309 to S315 is "H", the gate circuit 1308 outputs the inverted master signal 1024Mbar to the OR gate 1307 as an output signal S1308b.

- The OR gate 1307 outputs a rise-up signal S1307 to the gate terminal of the latch circuit 102 of the detect assistant pulse generating circuit 1 when any one of the input signals S1308a and S1308b is "H". The output start time of the detect assistant pulse signal is determined with the signal S1307 to alter the signal S1307, whereby alteration of the output start time of the detect assistant pulse signal can be realized.

Next, the operation of the circuit of this invention will be described with reference to a flowchart of Fig. 56.

- First, simultaneously with the start (2001), the initial setting (2034) is made to set the counter variable n to " $n = 0$ ". The main drive pulse P1 is set to $P1 = P0 + n\Delta P1$ (2023). At this time, P0 has the shortest pulse width (for example, $P0 = 1.95$ msec), n is set to 0 to 7, and $\Delta P1$ is set to 0.244 msec.

- After the setting of the main drive pulse P1, the main drive pulse P1 is output to the motor (2036), and the pulse width of a next detect assistant pulse Pa is selected (2043). The counter value n is used for the selection of the pulse width. If " $n < 6$ ", the output start timing ITPa of the detect assistant pulse Pa is set to " $ITPa = ITPa0$ " (2044), and the detect assistant pulse Pa is output (2046). On the other hand, if " $n \geq 6$ ", the output start timing ITPa is set to " $ITPa = ITPa1$ " (2045), and the detect assistant pulse Pa is output (2046).

In the next rotation detecting operation (2005), the rotation or non-rotation of the rotor is judged. The detection method uses the comparison between VTH and VRS. If $|VRS| \leq |VTH|$, the correction drive pulse P2 is output (2006), and the counter variable n is incremented as follows: " $n = n + 1$ " (2038), thereafter terminating the operation of the rotation of the rotor.

- 50 The above description is for the operating flowchart. P0, $\Delta P1$, ITPa0, ITPa1 can be easily determined on the electrical circuit, and these are not necessarily to be limited to the above pulse width.

(9) Ninth Embodiment

- 55 In the ninth embodiment of this invention, the detect assistant pulse is alternated, and then output to the motor. Figs. 57(a) to (d) are diagrams for the drive voltage waveform of the ninth embodiment.

There are various methods for generating an alternating pulse. The generation of the alternating pulse may be performed in the pulse generating circuit of the eighth embodiment and the other embodiments as

described above, and thus the description thereof is omitted from the following embodiment.

The alternating pulse as shown in Fig. 57(a) is an embodiment of an alternating pulse which is formed by a detect assistant pulse PaX to be applied in an opposite direction to the main drive pulse and a detect assistant pulse PaY to be applied in the same direction as the main drive pulse.

5 The alternating pulse as shown in Fig. 57(b) is an embodiment of an alternating pulse for intermittently applying the detect assistant pulses PaX and PaY.

The alternating pulse as shown in Fig. 57(c) is an embodiment of an alternating pulse obtained by reversing the application order of the detect assistant pulses PaX and PaY for the alternating pulse as shown in (a).

10 The alternating pulse as shown in Fig. 57(d) is an embodiment of an alternating pulse for applying the detect assistant pulse PaY to the stepping motor after plural detect assistant pulses PaX, for example, PaX1 and PaX2 are applied to the stepping motor. The same effect can be also obtained by providing plural detect assistant pulses PaY.

15 It can be easily realized that the alternating pulses as shown in Figs. 57(a) to (d) are repetitively applied to the stepping motor.

The effects of each embodiment disclosed in the present invention will be explained hereafter.

(Embodiment 1)

20 As described above, according to this invention, the rotation detecting system for the stepping motor in which the voltage induced in the coil of the stepping motor 7 after the interruption of the main drive pulse is converted to the transient voltage in the detecting circuit 6, thereby to electrically carry out detection judgment on the rotation of the stepping motor, the detect assistant pulse generating circuit 1 is provided on the circuit, and driving means for stepping motor for applying the detect assistant pulse as an effective power pulse from the driving circuit 5 after the interruption of the main drive pulse and before the detection of the rotation is provided.

25 The following effects can be obtained by the above construction in which the detect assistant pulse is provided before the rotation of the rotor is detected.

30 (1) When the main drive pulse having a wide pulse width and a large effective power is applied to the stepping motor in order to realize an accurate stepping operation by increasing the driving torque of the motor in accordance with unexpected increase of an external load torque, the output of the correction drive pulse due to an erroneous judgment operation which is caused by reduction of the induced voltage can be avoided, and the required minimum effective power can be supplied to the stepping motor.

35 (2) Even when a compact rotor, that is, a rotor having small inertia moment is used to realize miniaturization, thinning and low power-consumption for clocks, an erroneous judgment operation due to the stop of the rotation attenuating motion of the rotor after the interruption of the main drive pulse can be avoided, and the precision of the rotation detection can be effectively improved.

(3) High precision can be maintained for the rotation detection irrespective of dispersion in shape of parts of stepping motor due to mass production.

(Embodiment 2)

40 The detect assistant pulse output selecting circuit 10 for selecting whether the detect assistant pulse is output in accordance with the output result of the detecting circuit 6 obtained in the previous stepping operation is provided on the circuit of the embodiment 1. The following effect can be obtained by an electronic clock having the above construction in which the detect assistant pulse is output before the rotation detection of the rotor, and further the output or non-output is controlled.

45 (4) When the output or non-output of the detect assistant pulse is controlled in accordance with the rotation detection result of the rotor, the output of the detect assistant pulse is stopped in the stepping operation where the rotation detection is relatively stable, and thus the consumption of the effective power due to the detection assistant pulse can be prevented.

(Embodiment 3)

50 The detect assistant pulse width altering circuit 11 for altering the pulse width in accordance with the output result of the detecting circuit 6 obtained in the previous stepping operation is provided on the circuit of the first embodiment. The following effects can be obtained by an electronic clock having the construction in which the detect assistant pulse is output before the rotation detection of the rotor is carried out, and the pulse width is alterable.

55 (5) Even when the rotational motion of the rotor is moderated due to variation of a ring array load in accordance with time lapse and sudden increase of an external load torque, and the induced voltage required for the detection cannot be obtained, at least two kinds of detect assistant pulses serving as effective power are selected in accordance with the detection result and output to the stepping motor,

so that the adjustment of the rotation attenuating motion of the rotor can be made and the detection precision can be improved.

(6) The detect assistant pulse having the required minimum effective power is selected and output to the stepping motor, so that the rotation detection can be stabilized and the consumption of the power by the detect assistant pulse can be prevented.

(Embodiment 4)

The detect assistant pulse output counter 12 for counting the output of the detect assistant pulse is provided on the circuit of the second embodiment. The electronic clock thus constructed is effective for a ring array mechanism which periodically generates a load torque to the motor, for example, a clock with a calendar which has a jump-control spring for conducting an elastic jumping control on gears of a date wheel serving as a date indicating plate, for example.

(7) Even for a clock in which a load torque is periodically applied to a motor for a long time, for example in such a case where "the degree of moderation of the rotational motion of the motor is varied with time due to a load torque occurring in a date feeding operation", the output of the correction drive pulse due to the erroneous judgment and the consumption of current can be prevented through management of the output frequency of the detect assistant pulse such as an operation of outputting the detect assistant pulse until the load torque is reduced.

(Embodiment 5)

The detect assistant pulse output timing generating circuit 13 for altering the output start timing of the detect assistant pulse in accordance with the output result of the detecting circuit 6 obtained in the previous stepping operation is provided on the circuit of the first embodiment. According to the electronic clock having the construction that the detect assistant pulse is output before the rotation detection of the rotor is carried out, and the pulse width thereof is altered,

(8) The output of the detect assistant pulse can be met with the timing at which the rotational motion of the rotor is liable to be amplified, and thus it is effective to keep the rotation detection result stable at all times.

(Embodiment 6, Embodiment 7, Embodiment 8)

The main drive pulse generating circuit 3 for generating plural main drive pulse signals is provided on the circuit of the first embodiment, and as a method of controlling (a) the detect assistant pulse output selecting circuit 10 for selecting whether the detect assistant pulse is output, (b) the detect assistant pulse width altering circuit 11 for altering the pulse width of the detect assistant pulse, and (c) the detect assistant pulse output timing generating circuit 13 for altering the output start timing of the detect assistant, the control is made in accordance with the signal of the main drive pulse generating circuit 3, so that:

(9) the number of the elements to be added to the circuit, and the circuit size can be miniaturized.

(Embodiment 9)

The alternating pulse has an effect on the improvement of the induced voltage required for the rotation detection of the rotor (by PaX), and on the control for preventing disorder of the rotor (a phenomenon that the rotor runs over a normal rest angular position, and rotates to a next rest angular position)(pulse PaY). The disorder of the rotor occurs when the driving voltage of the motor is high (a power source having high voltage, such as a lithium cell or the like).

Industrial Applicability

As described above, the detect assistant pulse of this invention has great effects for stepping motors which are required to be miniaturized and thinned in construction, and have parts for which low current-consumption and high detection precision are required.

Claims

1. An electronic timepiece having a dividing circuit (8) for receiving a signal from an oscillating circuit (9) and a stepping motor (7) for transmitting rotation to a gear train including a detect assistant pulse generating circuit (1) for generating at least one detect assistant pulse signal which is such an effective power pulse that said stepping motor (7) is not rotated by one step, on the basis of a clock signal input from said dividing circuit (8), and outputting the generated pulse to a drive pulse selecting circuit (4), a main drive pulse generating circuit (3) for generating at least one kind of main drive pulse signal on the basis of the clock signal input from said dividing circuit (8) and outputting the generated pulse signal to said drive pulse selecting circuit (4), a correction drive pulse generating circuit (2) for generating a

- correction drive pulse signal longer than the main drive pulse on the basis of the clock signal input from said dividing circuit (8) and outputting the generated correction drive pulse signal to said drive pulse selecting circuit (4), said drive pulse selecting circuit (4) for selecting the output or non-output of the correction drive pulse signal in accordance with the main drive pulse signal, the detect assistant pulse signal and a detection signal from a detecting circuit (6) and outputting the main drive pulse signal, the detect assistant pulse signal and the correction drive pulse signal to a driving circuit (5), said driving circuit (5) for converting the main drive pulse signal, the detect assistant pulse signal and the correction drive pulse signal input from said drive pulse selecting circuit (4) to effective power pulses and outputting the effective power pulses to said stepping motor (8), and said detection circuit for carrying out a circuit switching operation on the basis of the clock signal input from said dividing circuit (8) to detect the rotation of said stepping motor (7) and generating a detection signal in accordance with a rotation detection result to output the detection signal to said detecting circuit (6).
2. The electronic timepiece as claimed in claim 1, further including a detect assistant pulse output selecting circuit (10) for making a selection as to whether the detect assistant pulse signal input from said detect assistant pulse generating circuit (1) is output to said drive pulse selecting circuit (4), on the basis of a signal obtained by compositing the detection signal of said detecting circuit (6) which is generated in accordance with the rotation result of a rotor in a previous stepping operation and the correction drive pulse signal.
 3. The electronic timepiece as claimed in claim 1, further including a detect assist pulse width altering circuit (11) for selecting one clock signal on the basis of at least two kinds of clock signals input from said dividing circuit (8) in accordance with the composite signal of the detection signal of said detecting circuit (6) and the correction drive pulse signal so that the pulse width of the detect assistant pulse is alterable, and outputting the selected clock to said detect assistant pulse generating circuit (1), wherein said detect assistant pulse generating circuit (1) generates the detect assistant pulse signal on the basis of the clock signal input from said detect assistant pulse width altering circuit (11) and said dividing circuit (8).
 4. The electronic timepiece as claimed in claim 2, further including a detect assistant pulse output counter (12) for counting the output frequency of the detect assistant pulse signal output from said detect assistant output selecting circuit (10) to said drive pulse selecting circuit (4), and outputting to said detect assistant pulse output selecting circuit (10) a counter signal for controlling an output selecting operation of said detect assistant pulse output circuit (10).
 5. The electronic timepiece as claimed in claim 1, further including a detect assistant pulse output timing generating circuit (13) for selecting a clock signal for altering an output start timing of the detect assistant pulse on the basis of the clock signal input from said dividing circuit (8) in accordance with the composite signal between the correction drive pulse signal and the detection signal of said detecting circuit (6) which is generated in accordance with the rotation detection result of said rotor in the previous stepping operation.
 6. The electronic timepiece as claimed in claim 1, further including a detect assistant pulse output selecting circuit (10) for making a selection as to whether the detect assistant pulse signal is output to said drive pulse selecting circuit (4) in accordance with at least one kind of signal input from said main drive pulse generating circuit (3).
 7. the electronic timepiece as claimed in claim 1, further including a detect assistant pulse width altering circuit (11) for selecting a clock signal to be output to said detect assistant pulse generating circuit (1) in accordance with at least one kind of signal input from said main drive pulse generating circuit (3).
 8. The electronic timepiece as claimed in claim 1, further including a detect assistant pulse output timing altering circuit (13) for selecting a clock signal for altering the output start timing of the detect assistant pulse on the basis of the clock signal input from said dividing circuit (8) in accordance with at least one kind of signal input from said drive pulse generating circuit (3).
 9. The electronic timepiece as claimed in any one of claims 1 to 8, wherein the detect assistant pulse to be applied to said stepping motor (7) is at least one alternating pulse.

FIG. 1

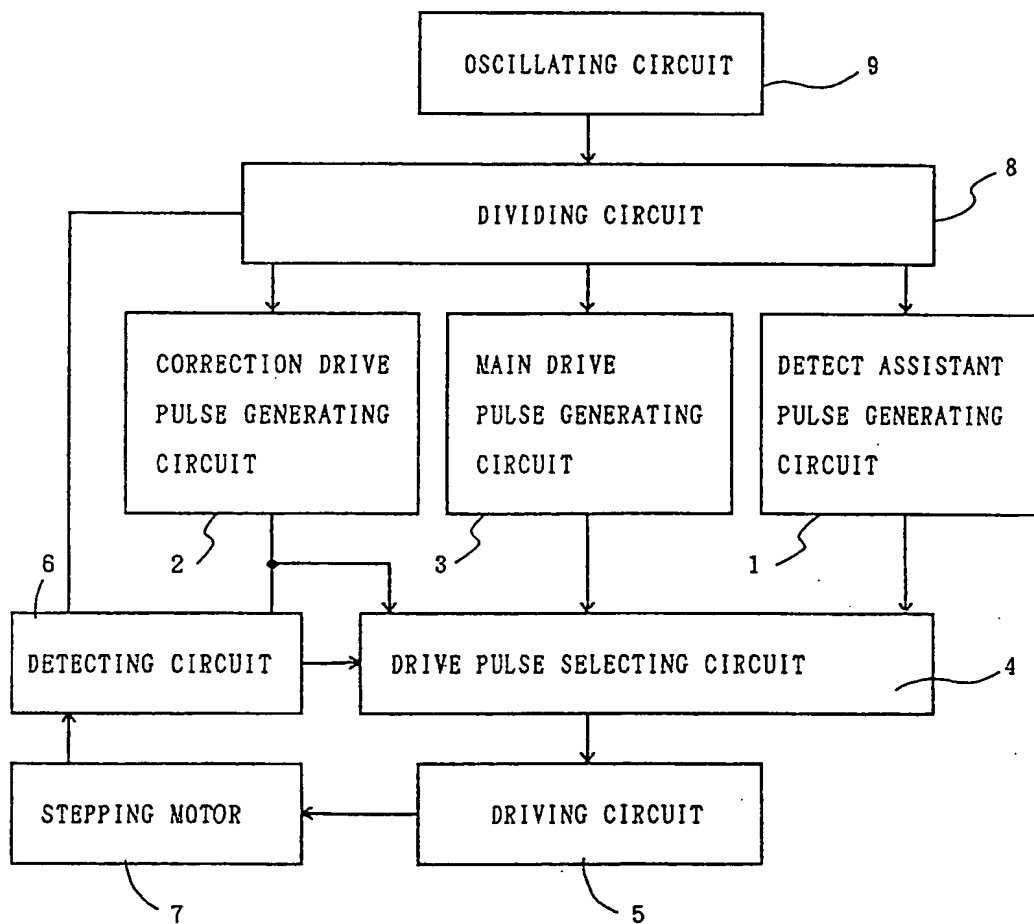


FIG. 4

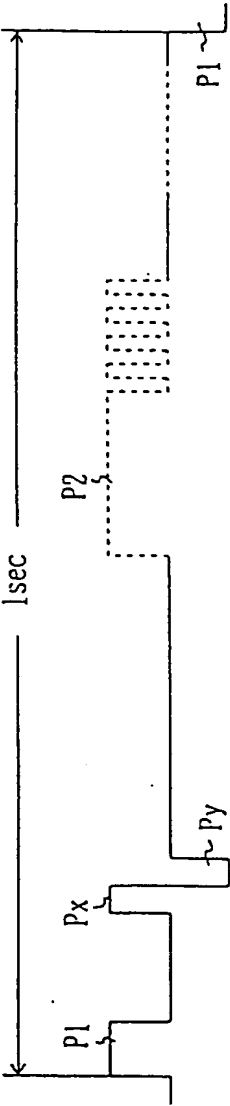


FIG. 5

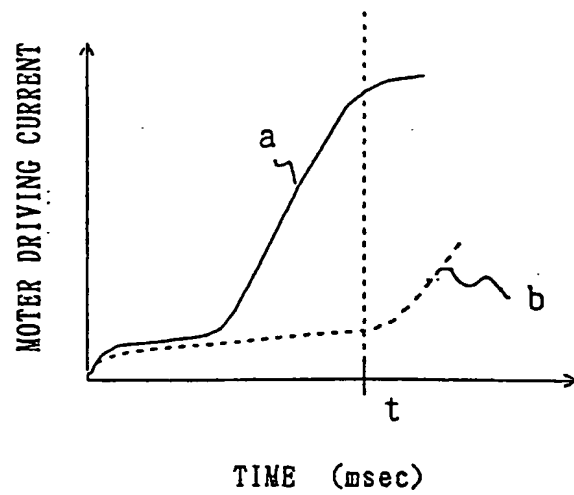


FIG. 6

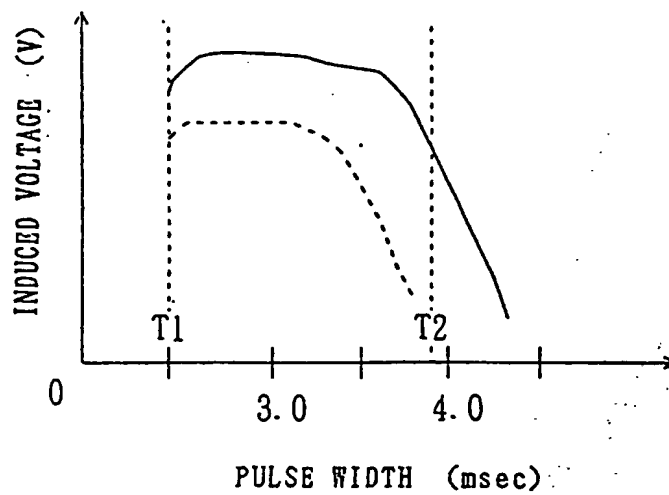


FIG. 7

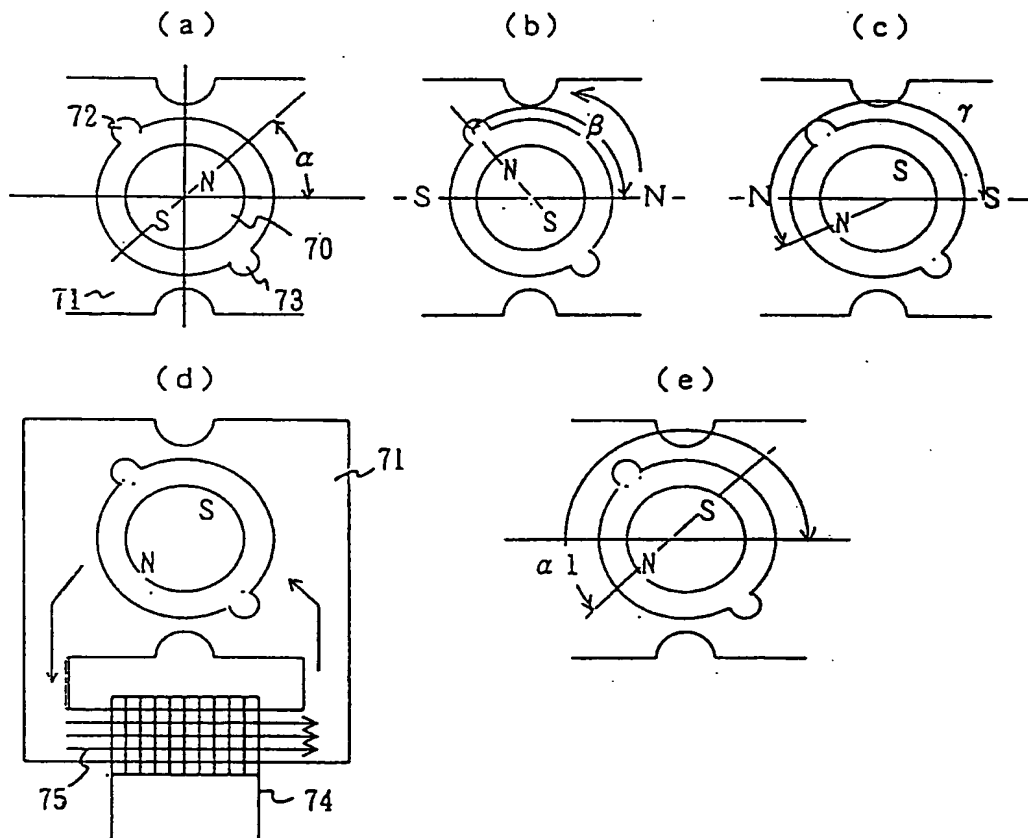


FIG. 8

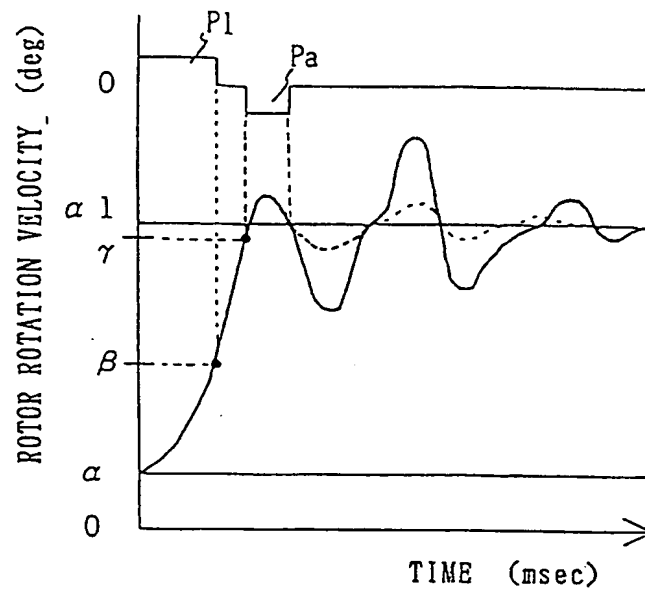


FIG. 9

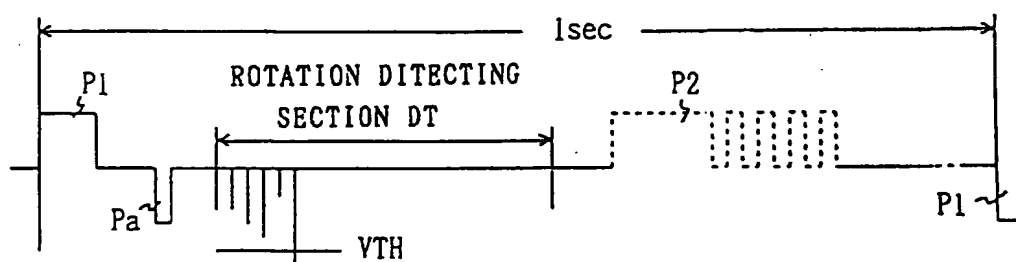


FIG. 10

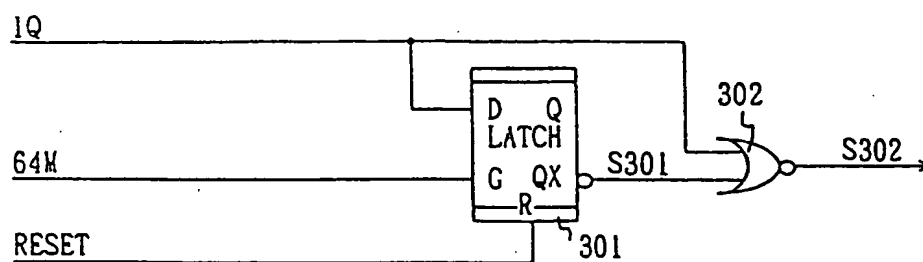


FIG. 11

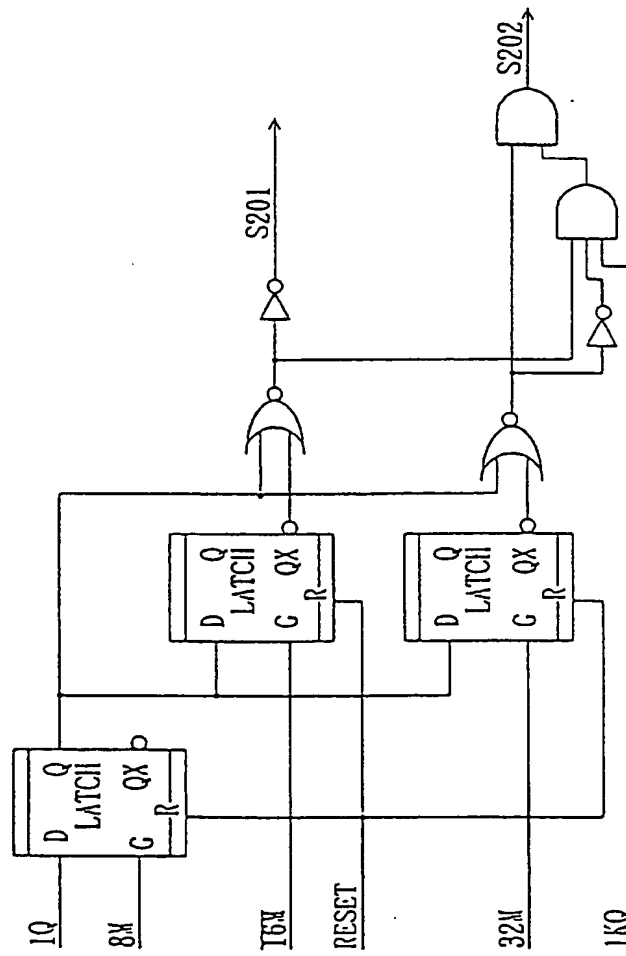


FIG. 12

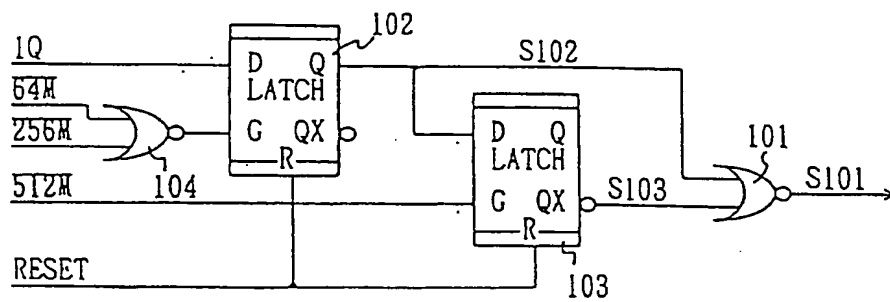


FIG. 13

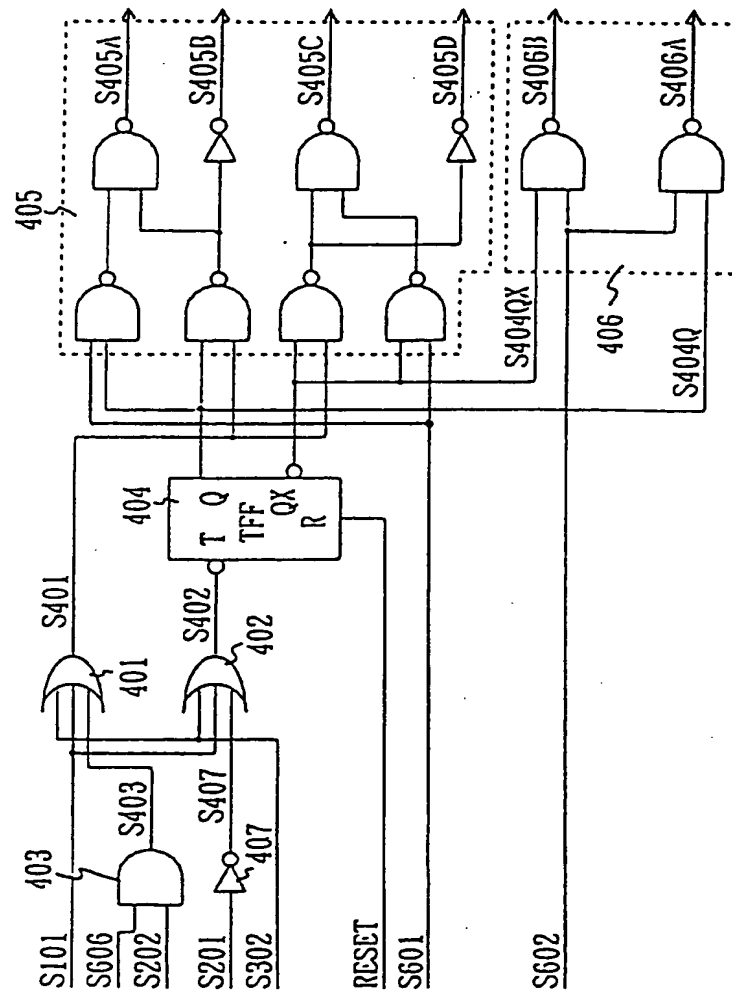


FIG. 14

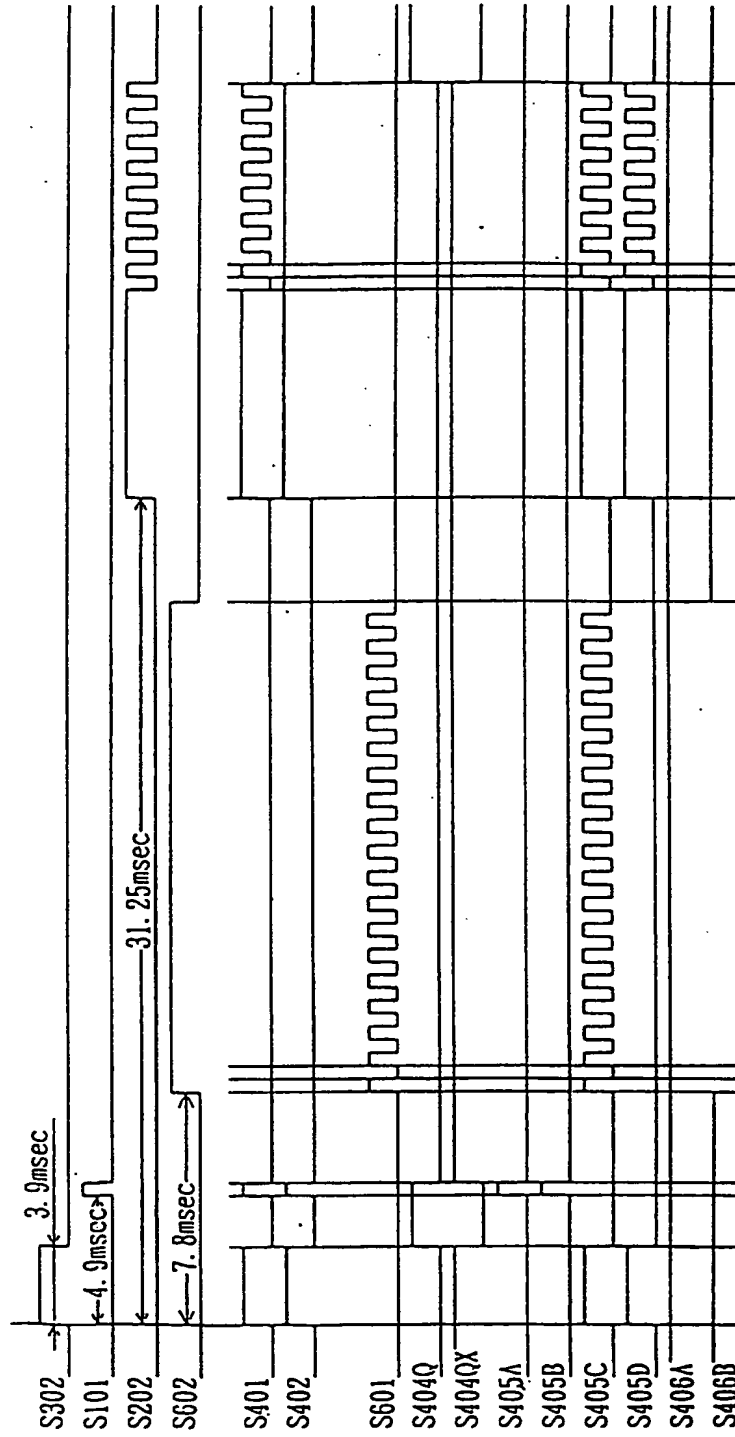




FIG. 17

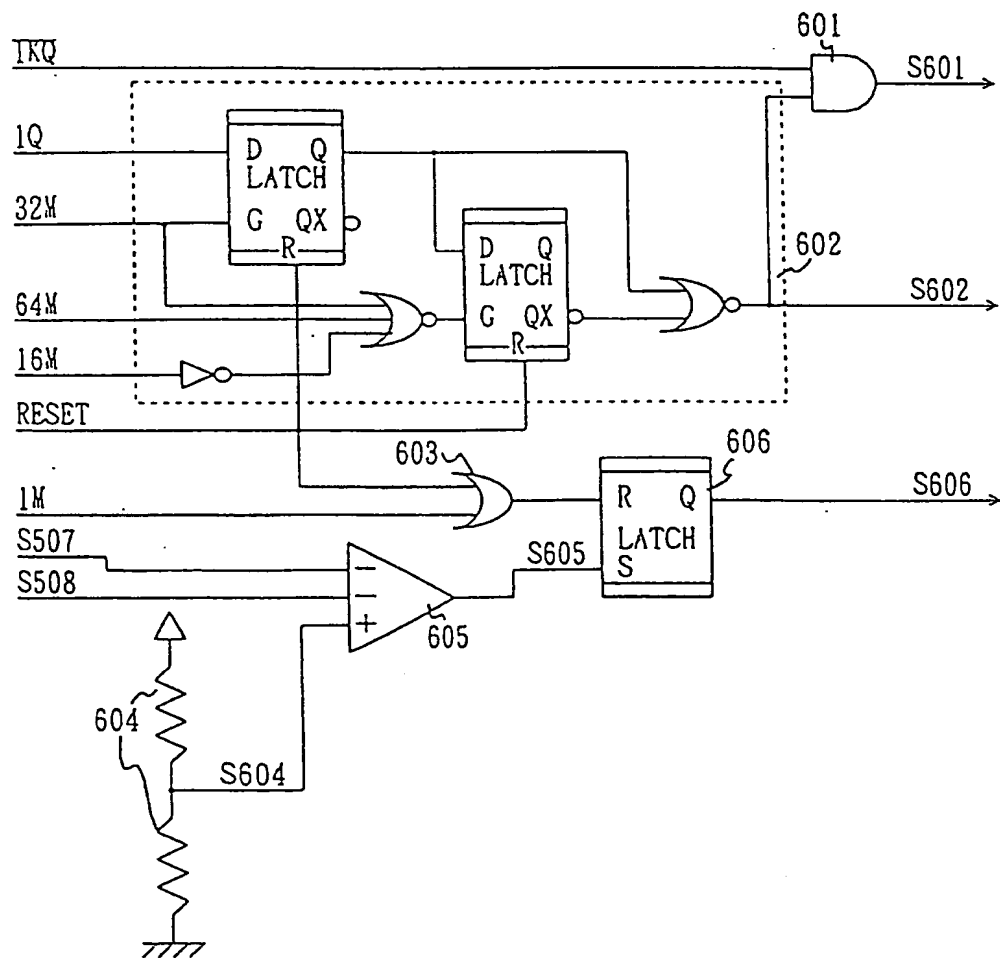


FIG. 18

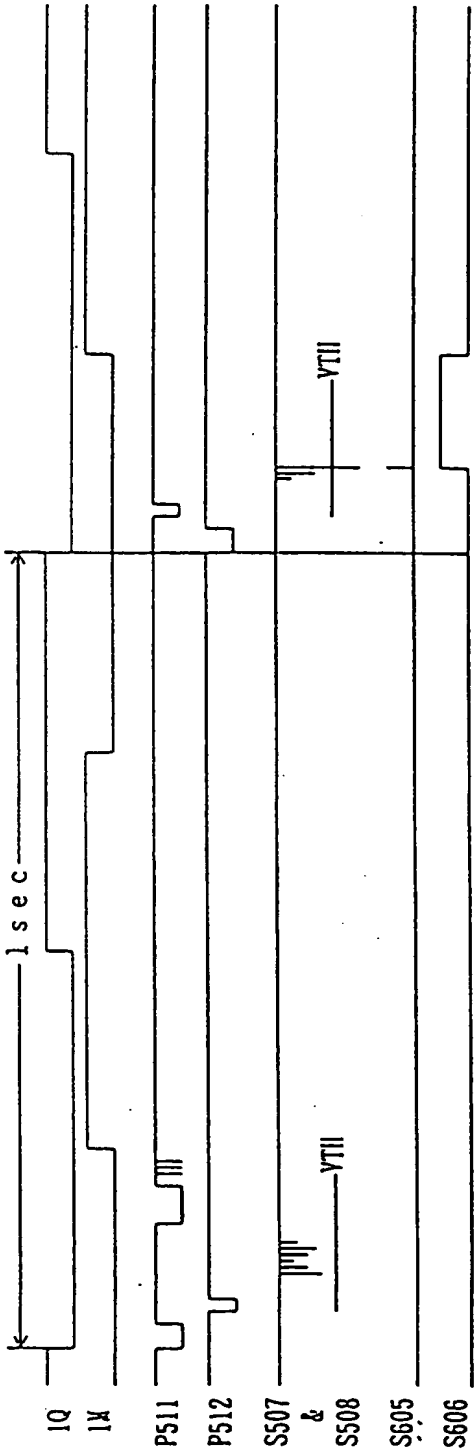


FIG. 19

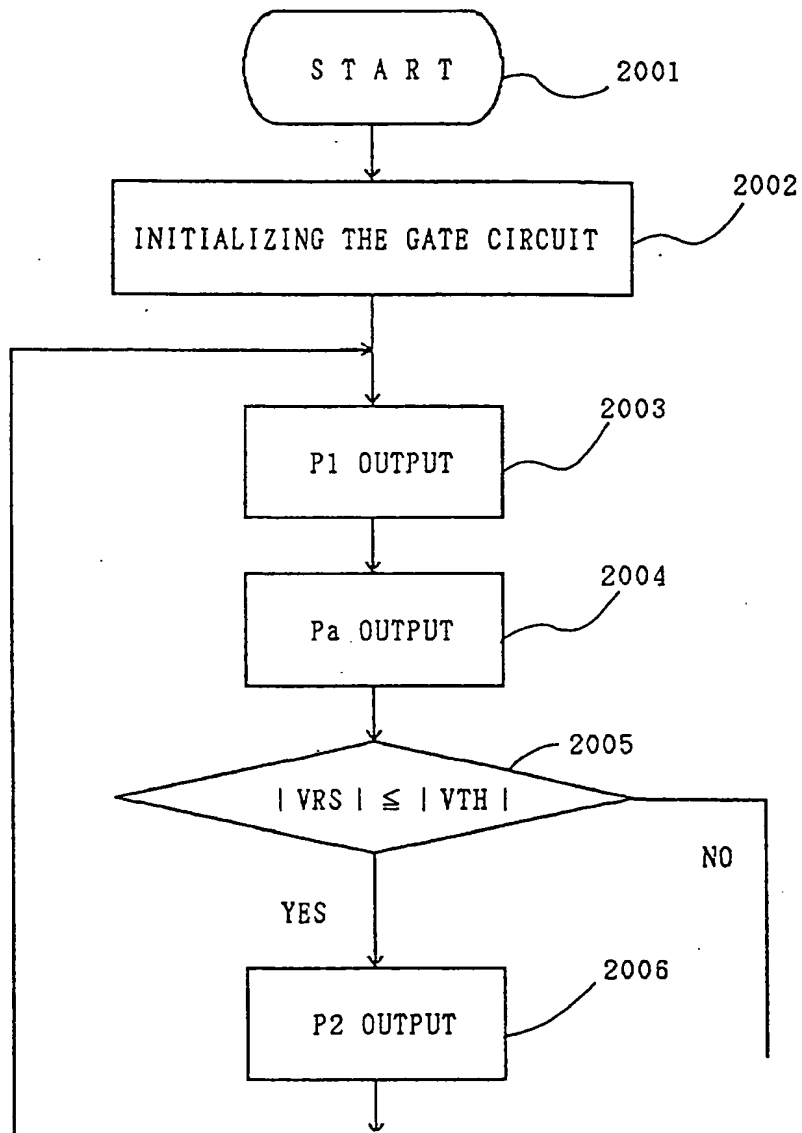


FIG. 2.0

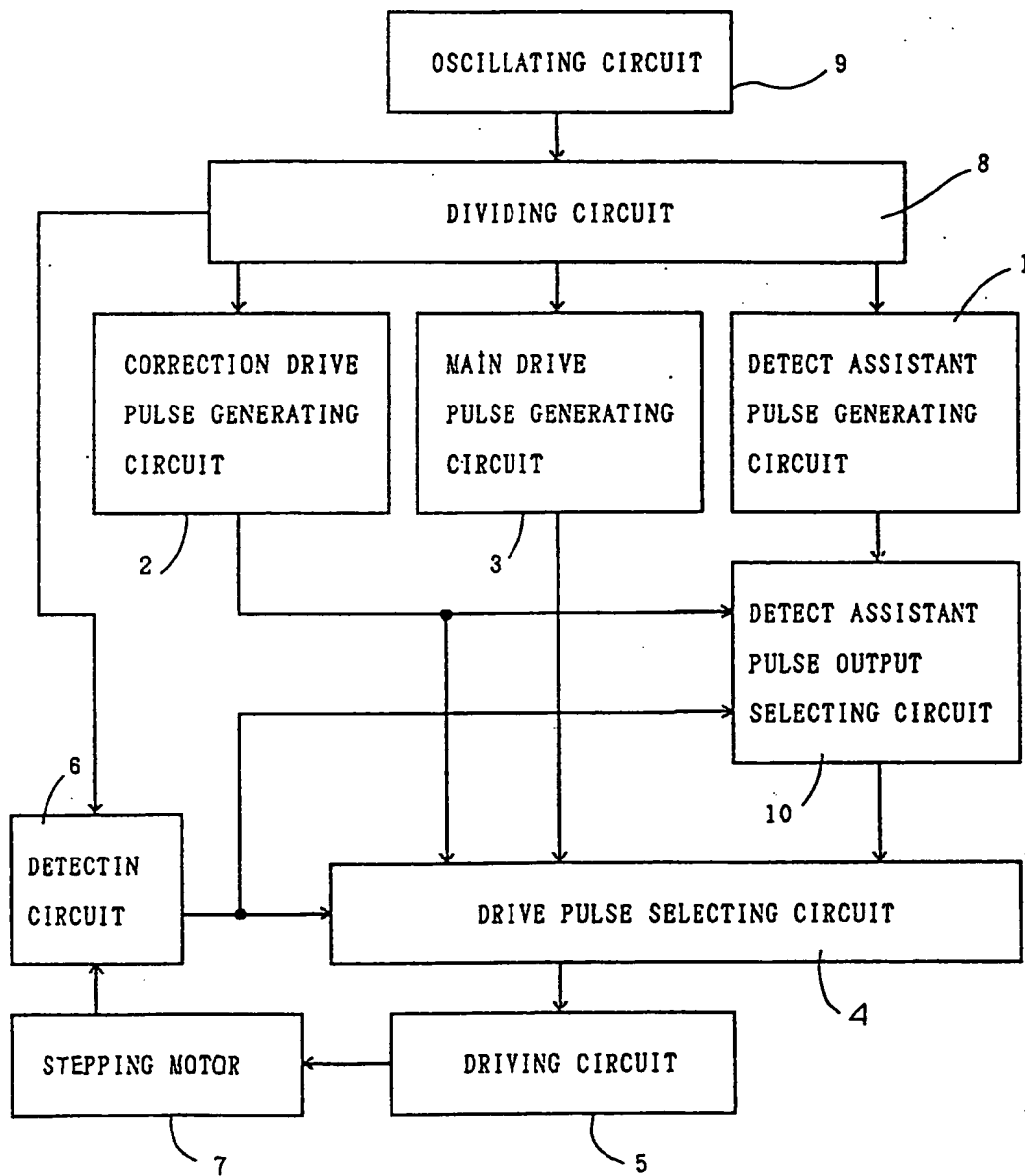


FIG. 21

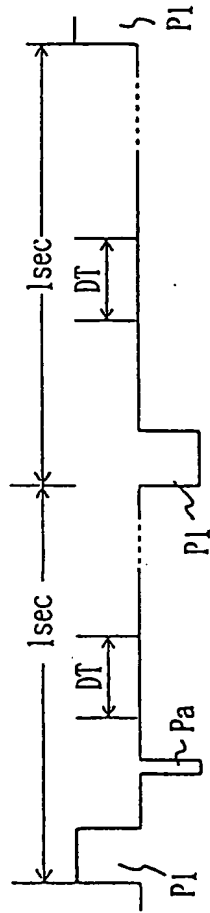


FIG. 22

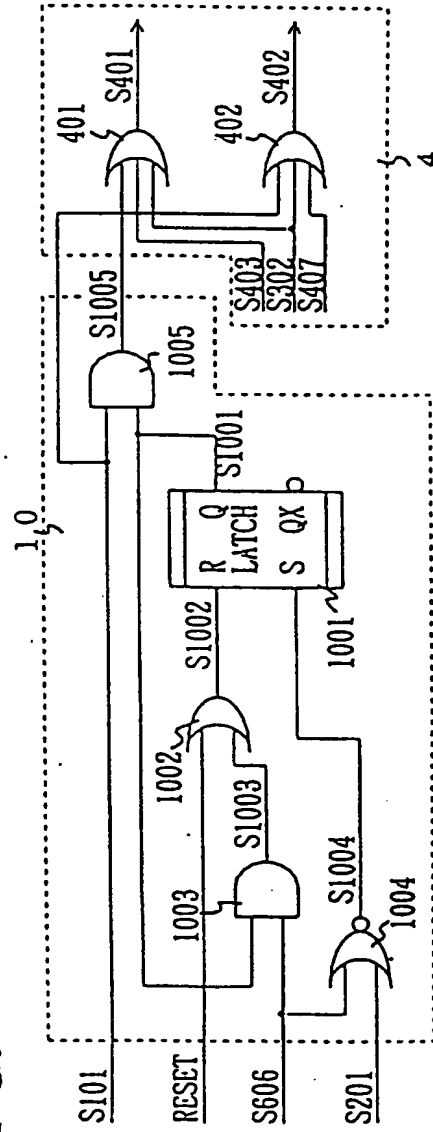


FIG. 23

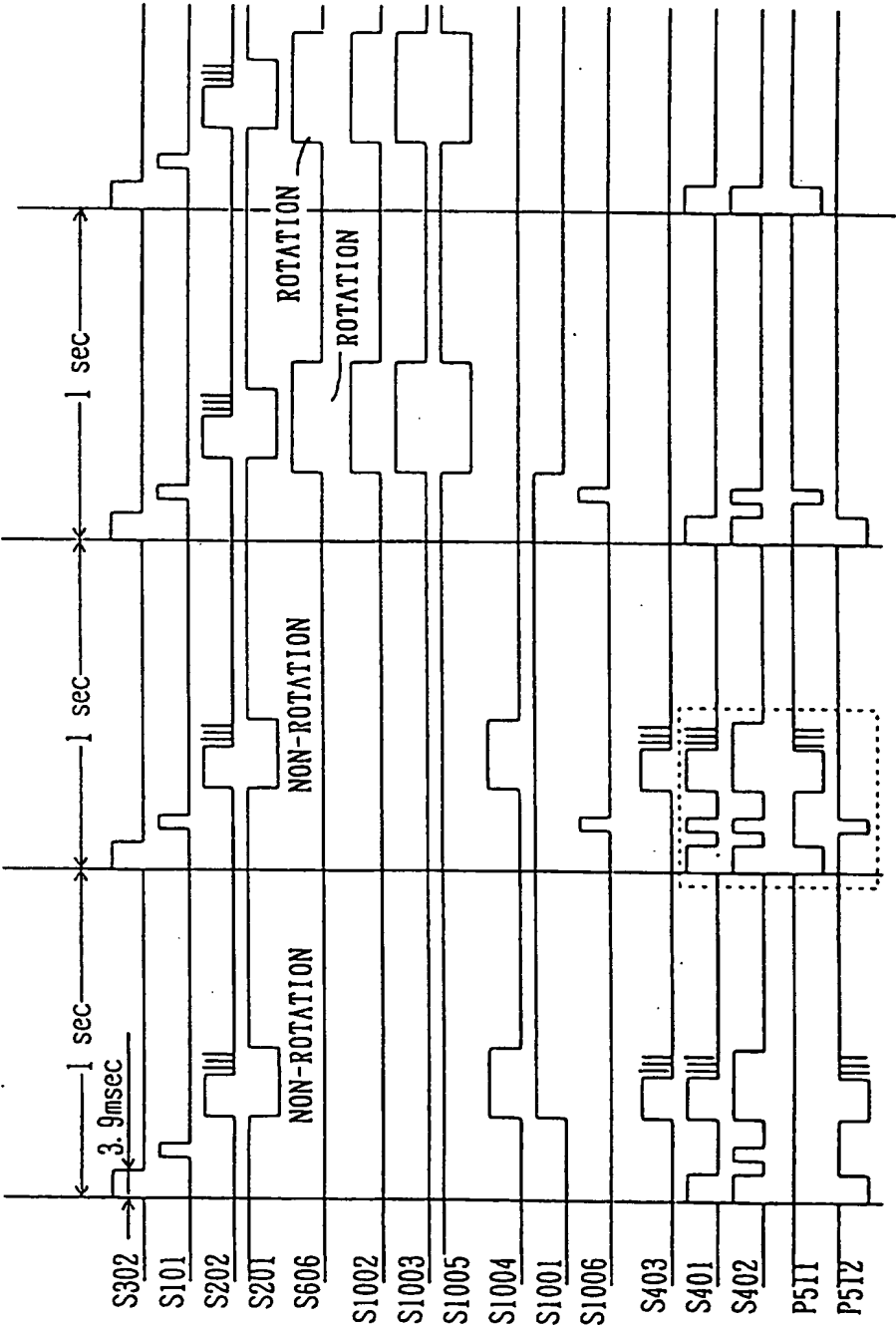


FIG. 24

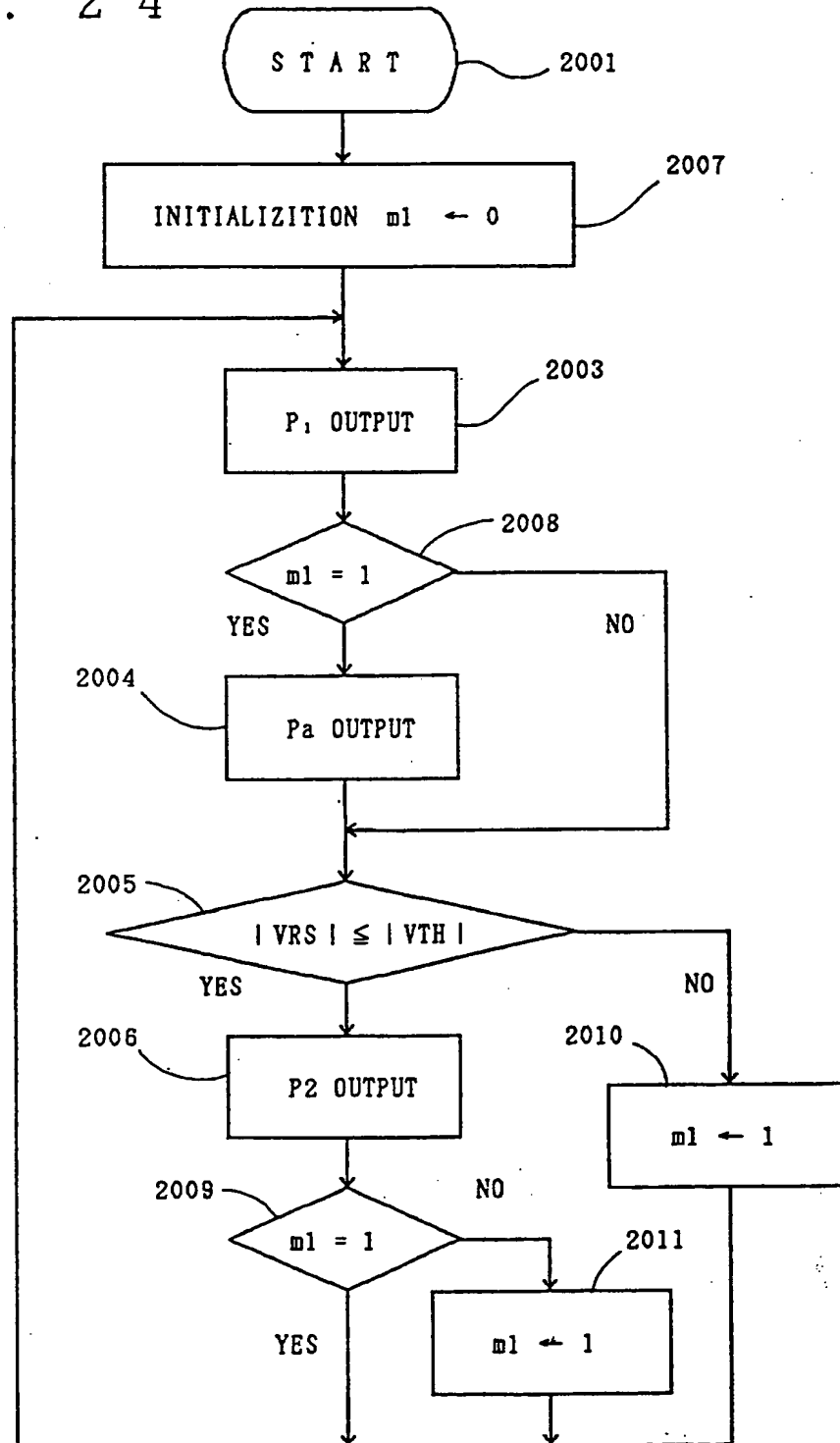


FIG. 25

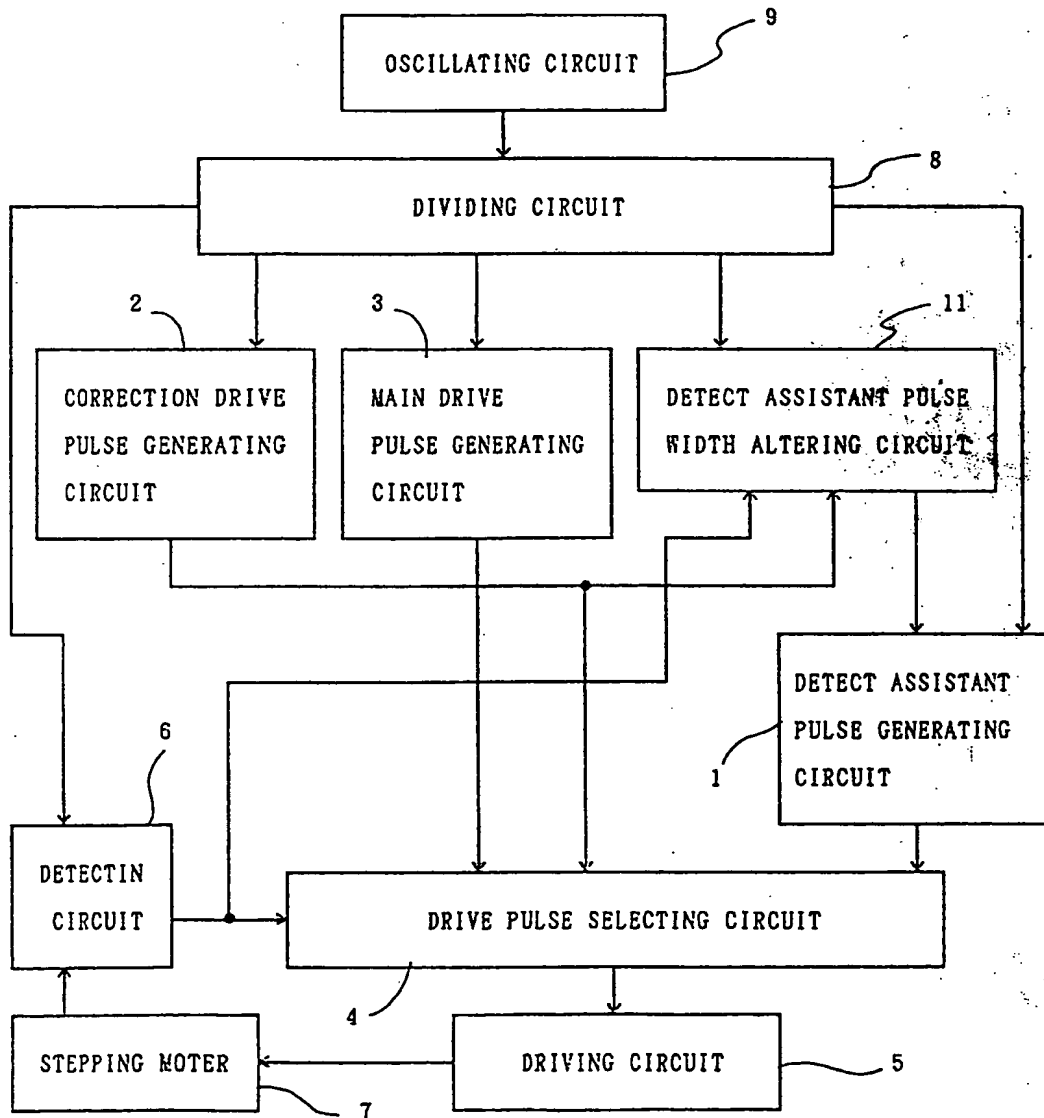


FIG. 26

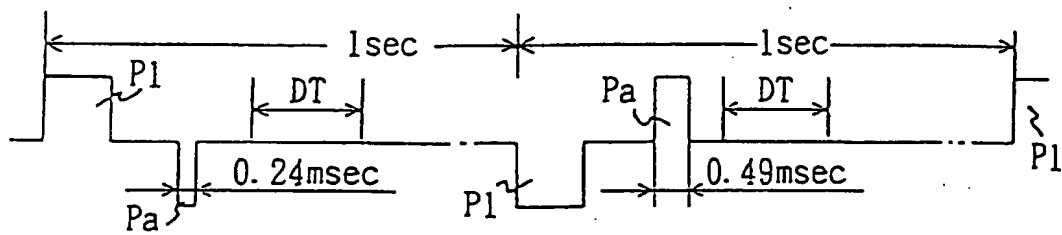


FIG. 27

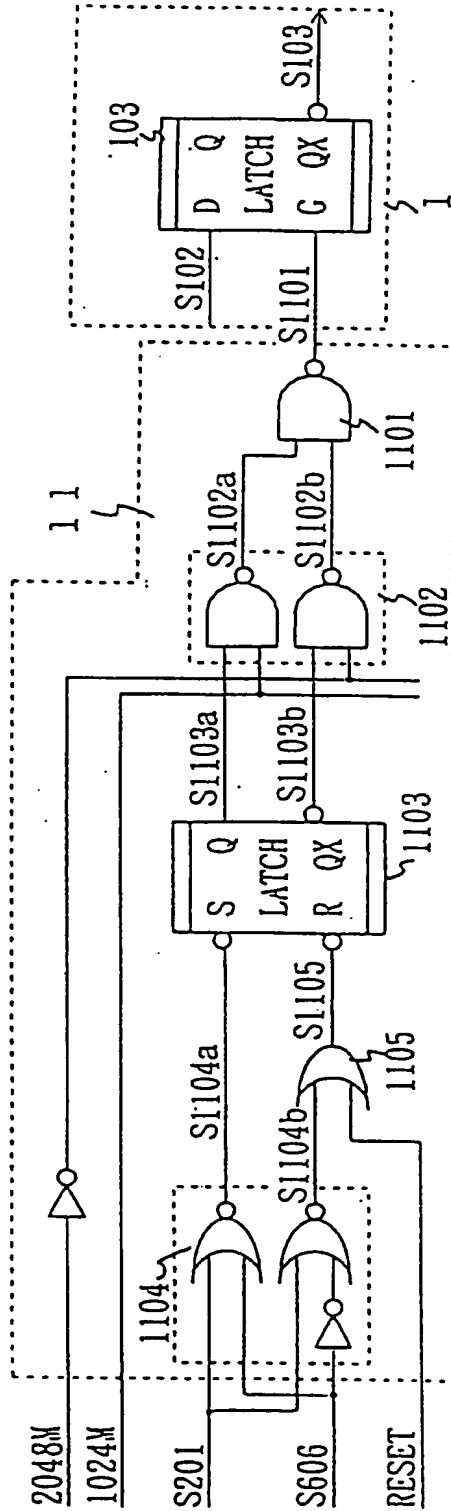


FIG. 28

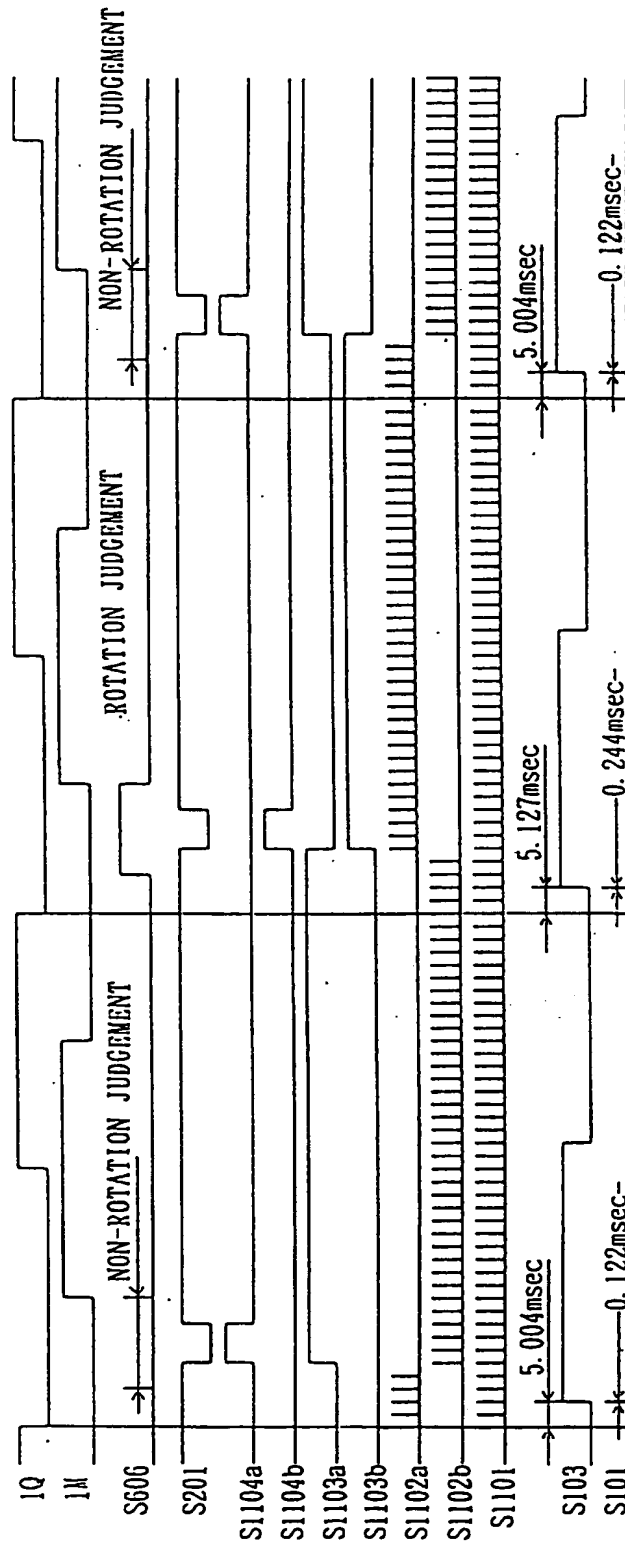


FIG. 29

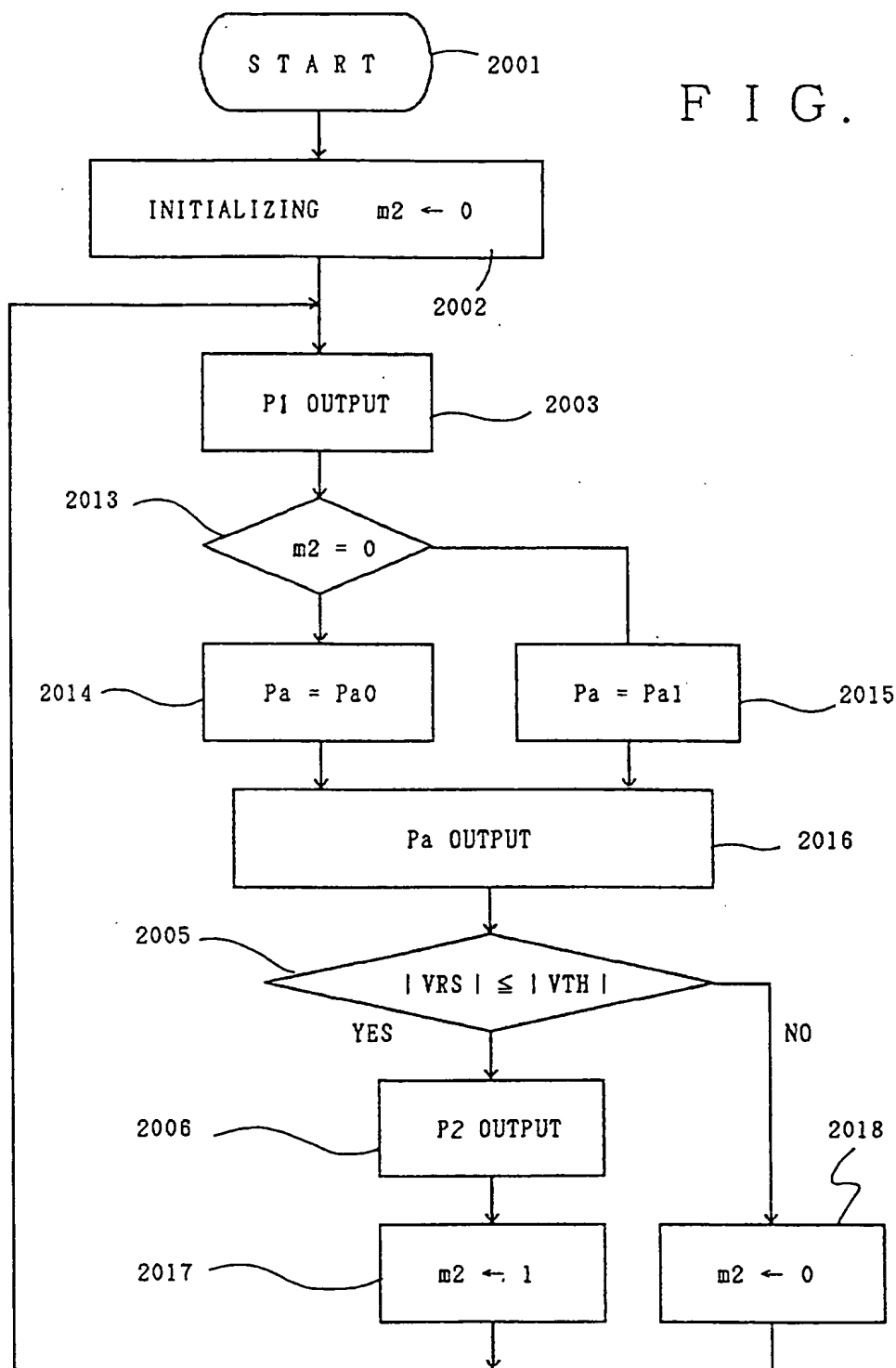


FIG. 30

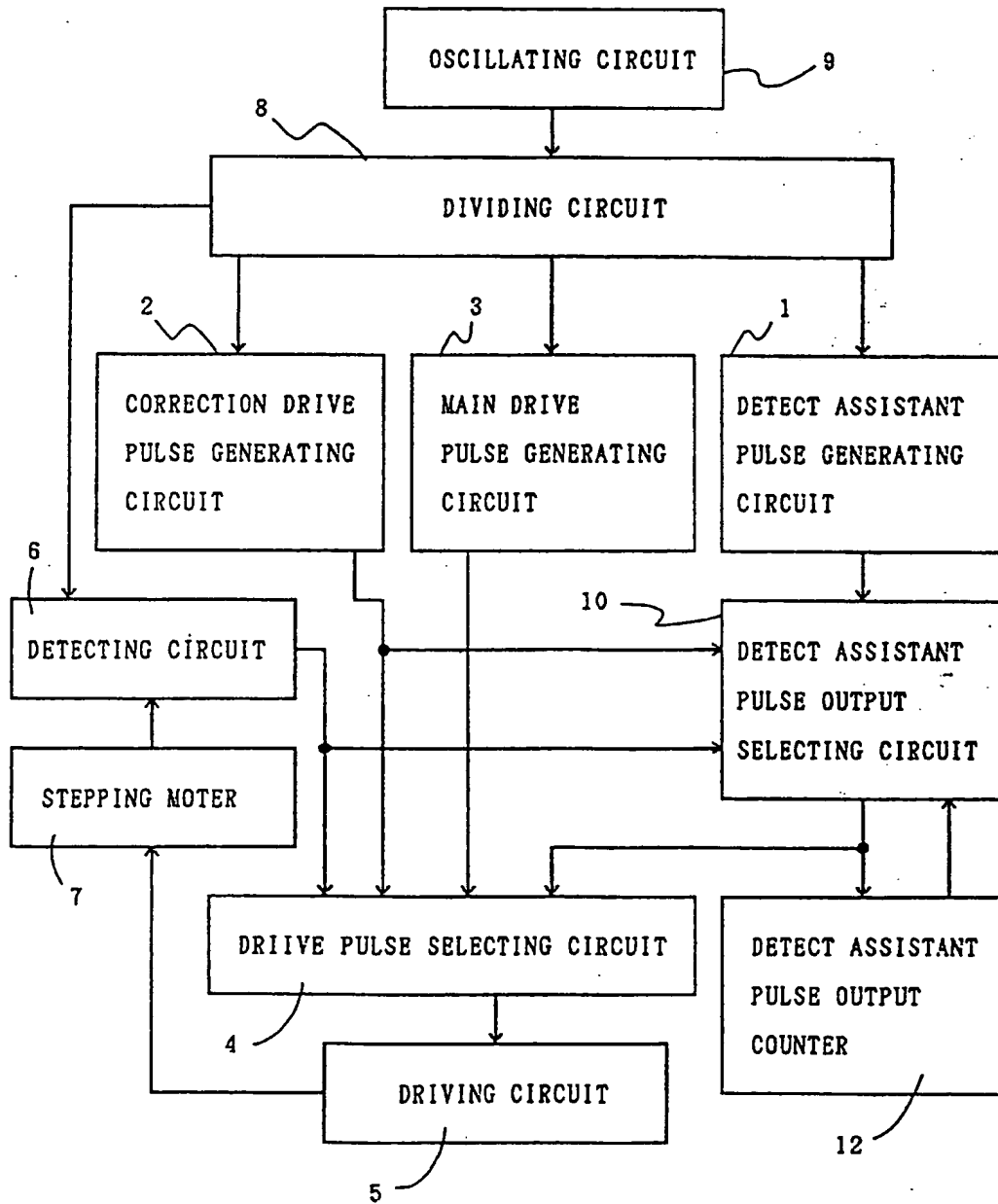


FIG. 31

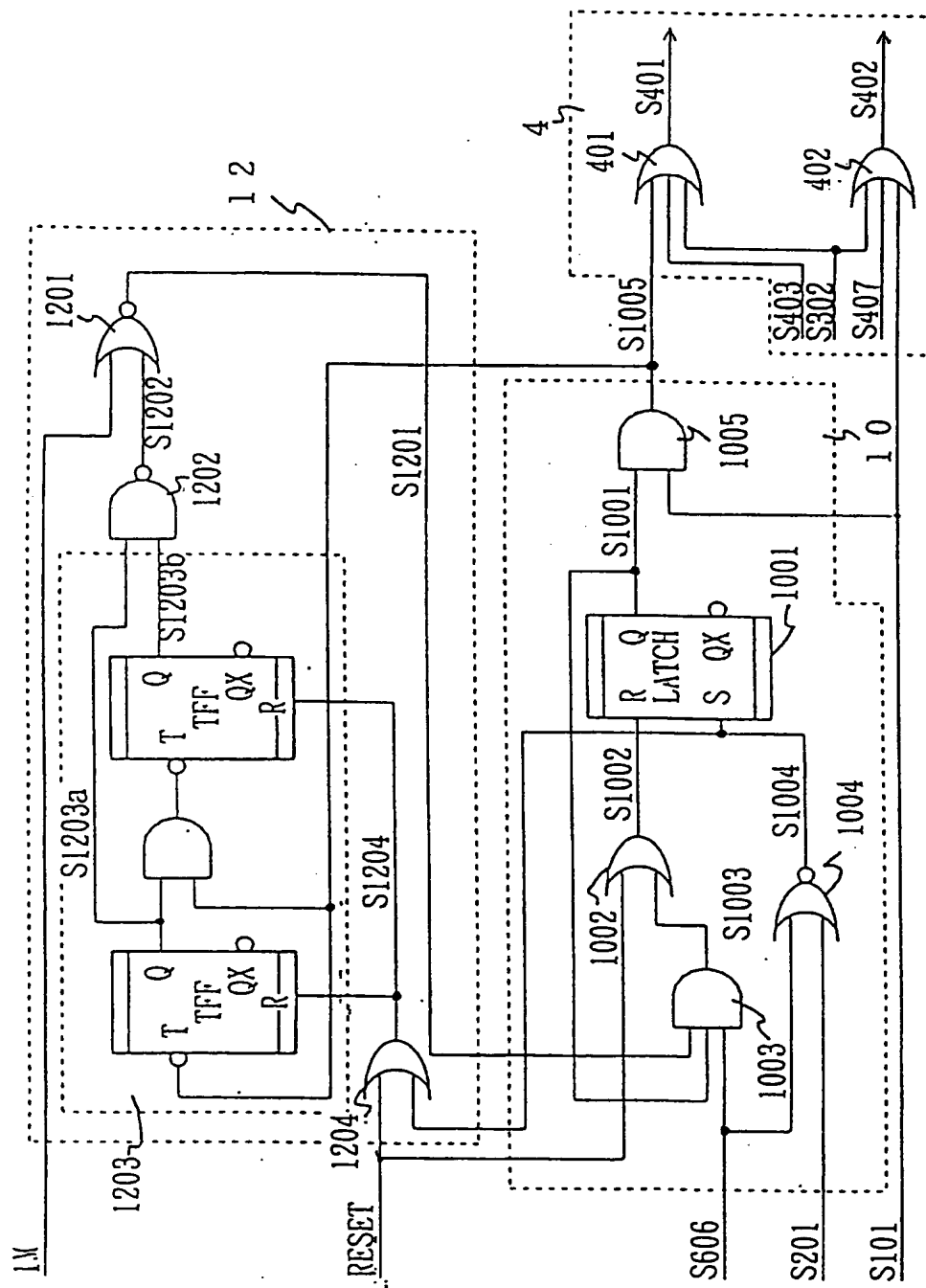
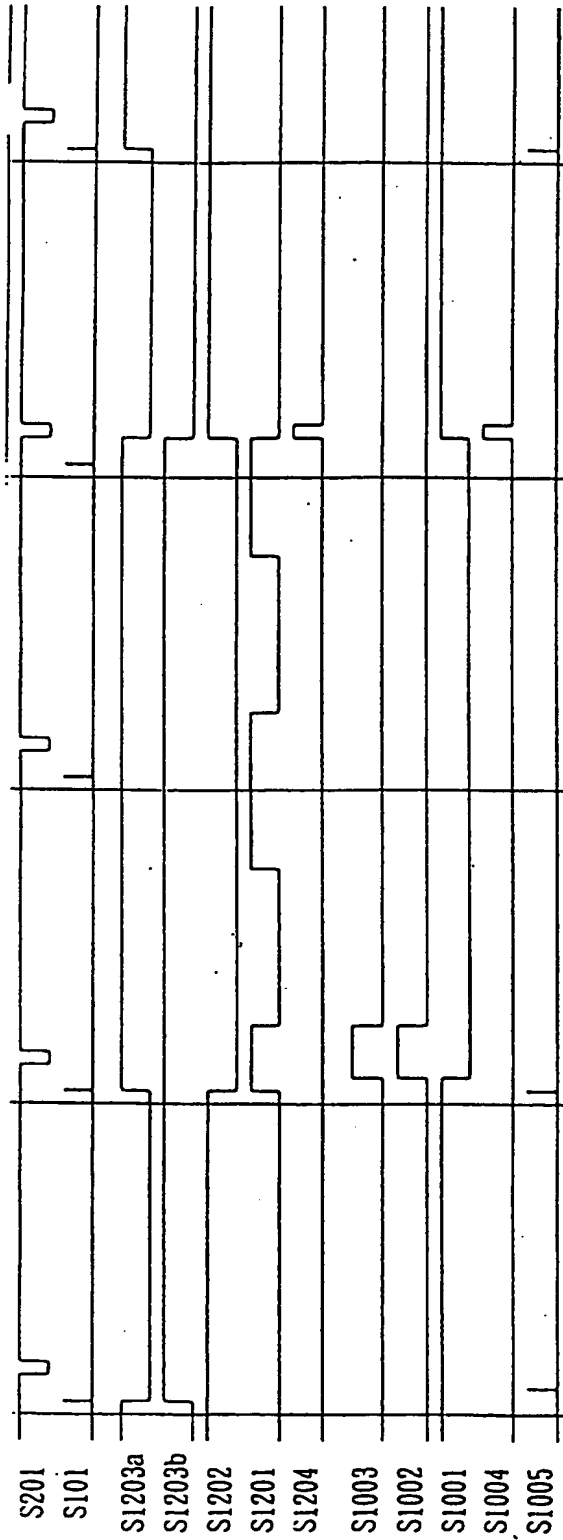


FIG. 32



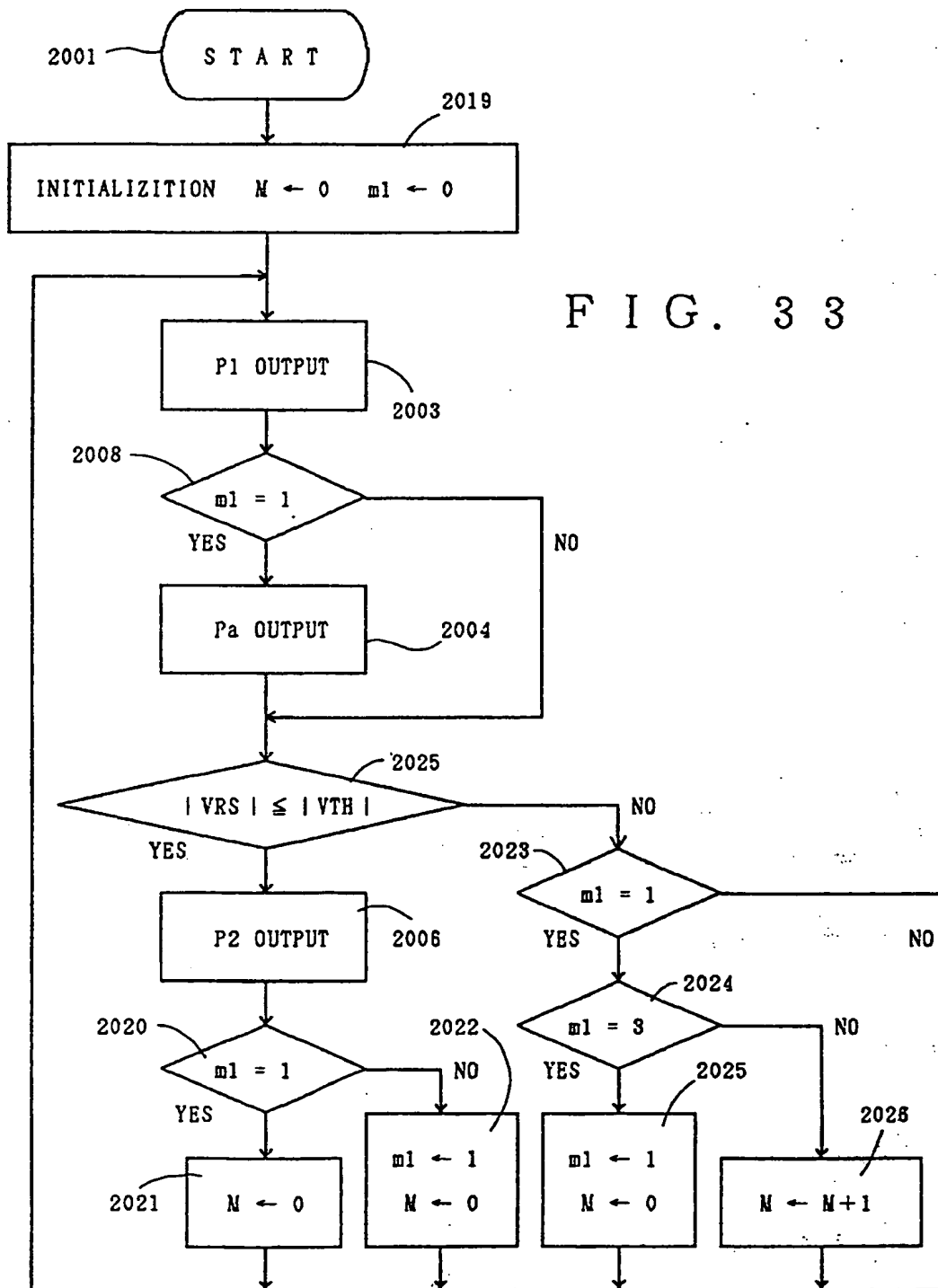


FIG. 34

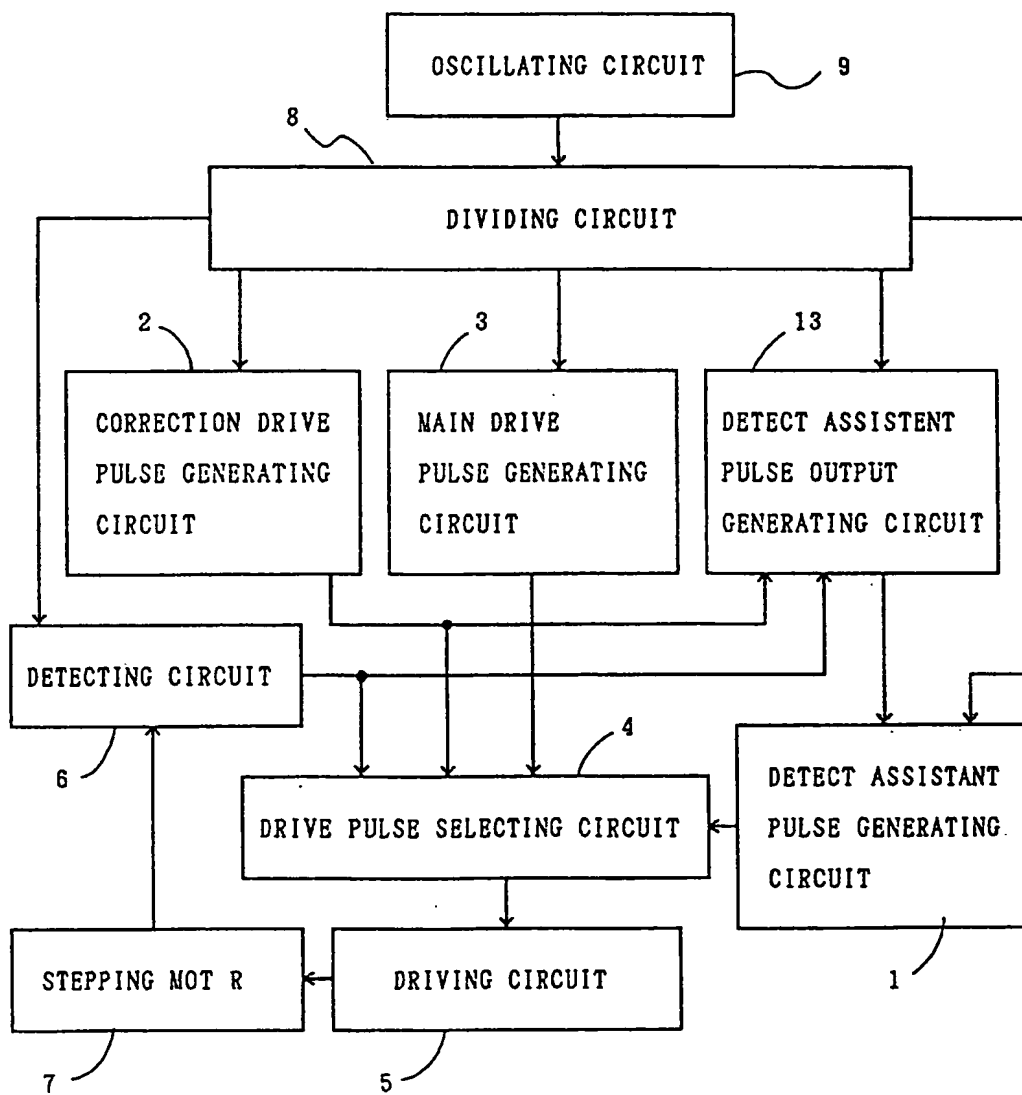


FIG. 35

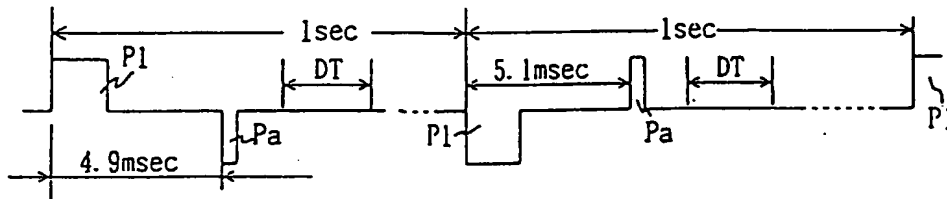


FIG. 36

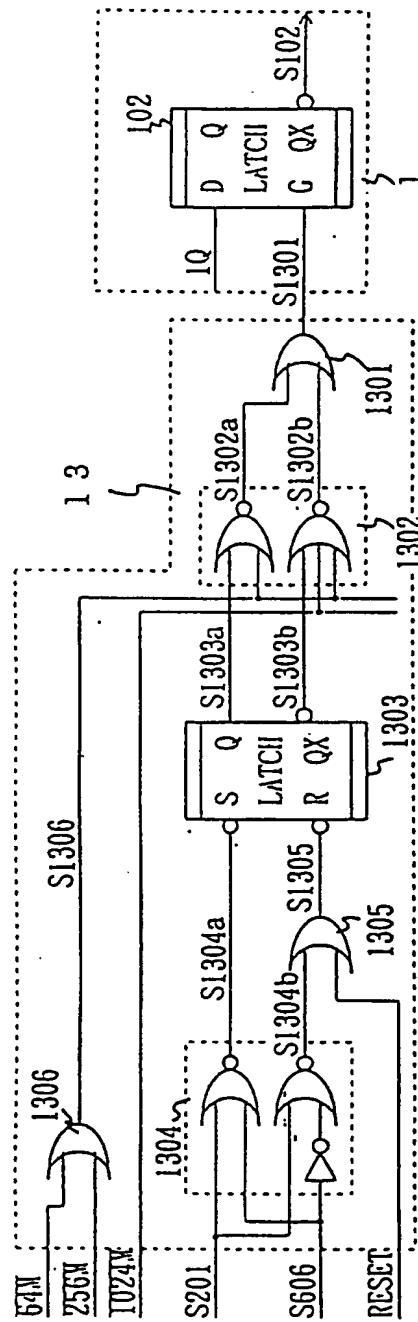
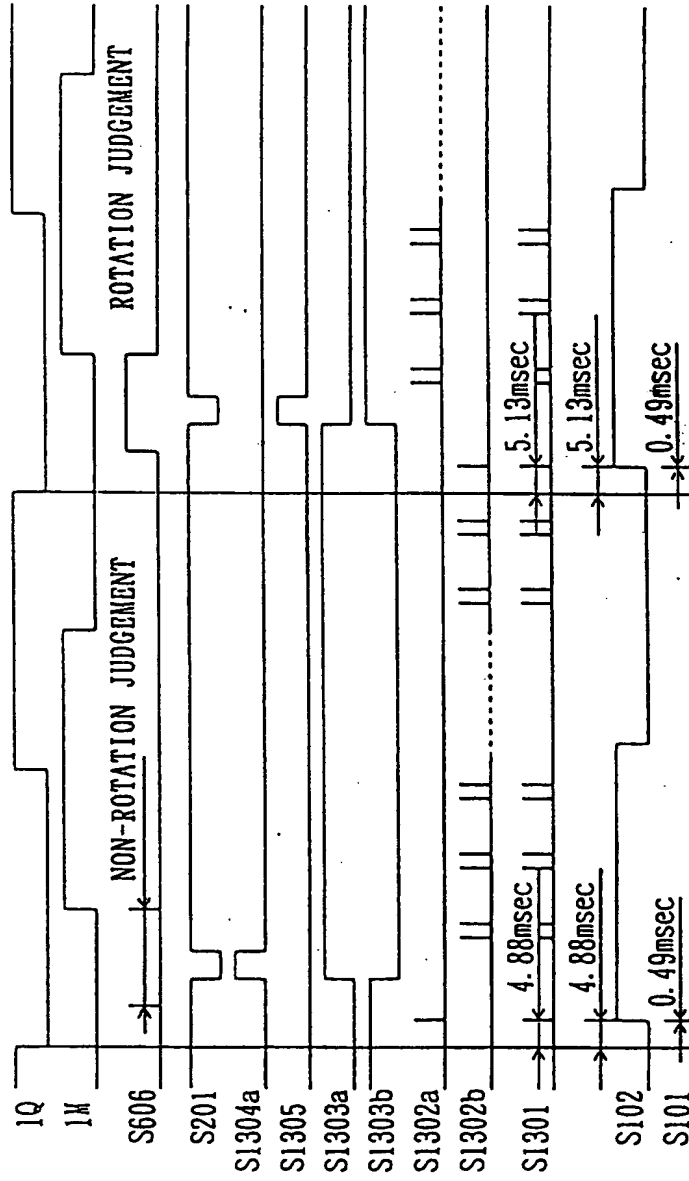


FIG. 37



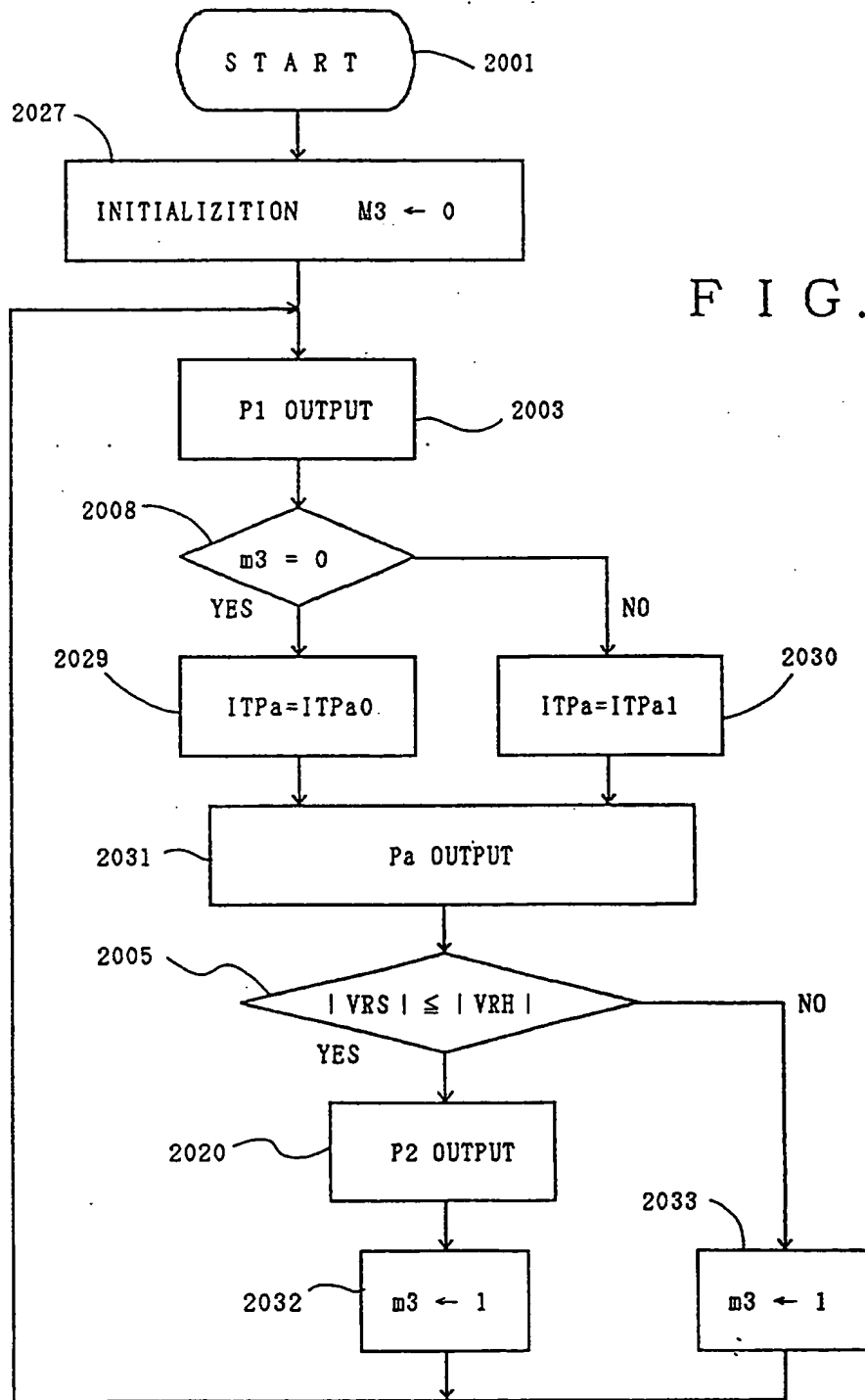


FIG. 38

FIG. 39

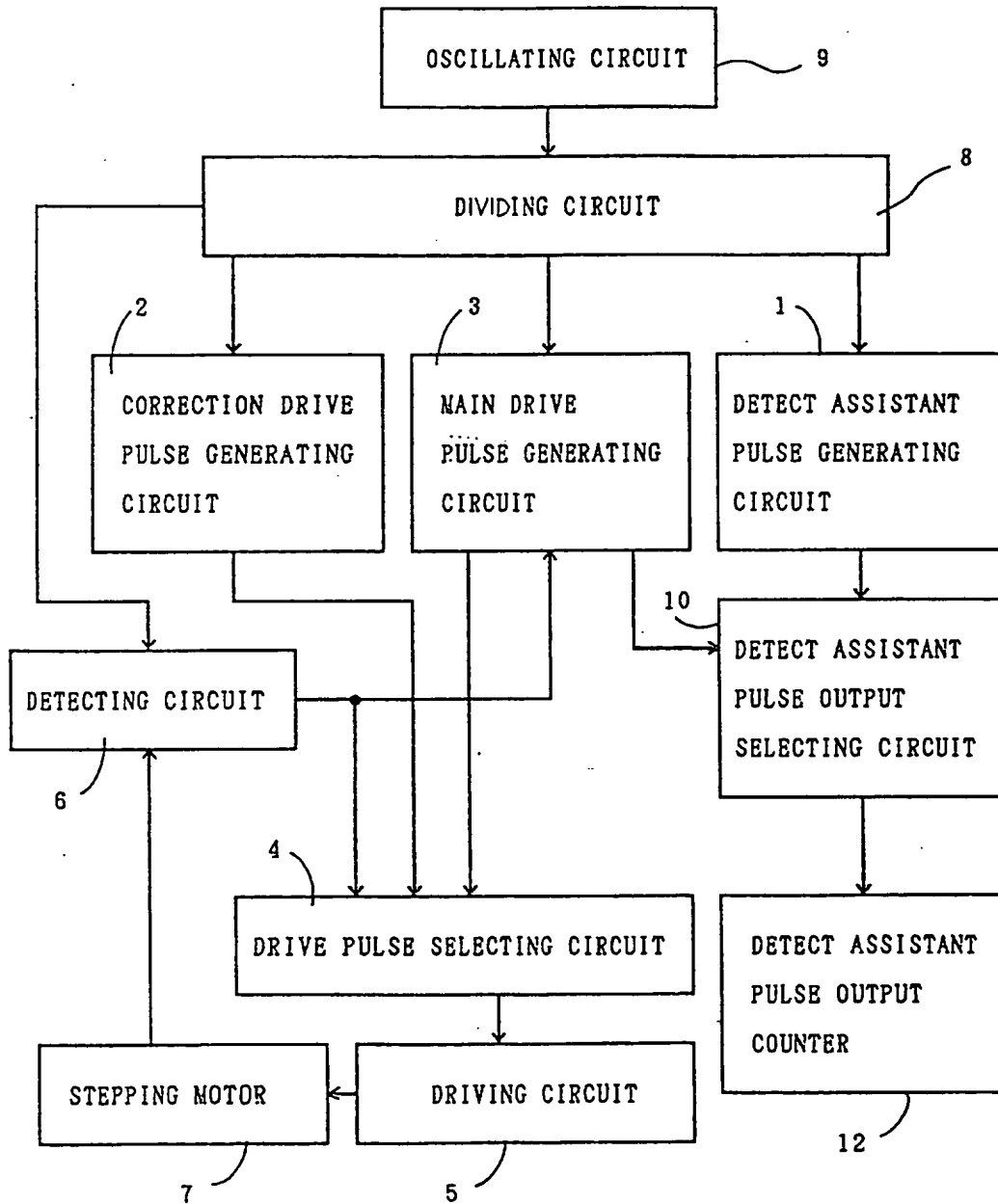


FIG. 40

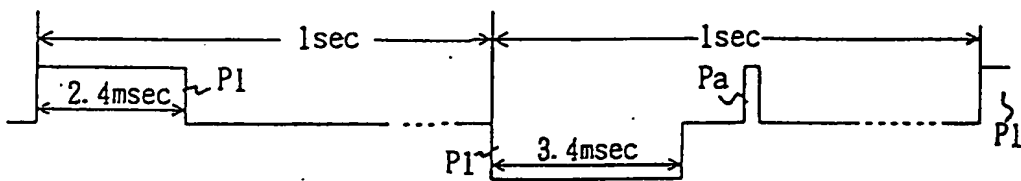


FIG. 41

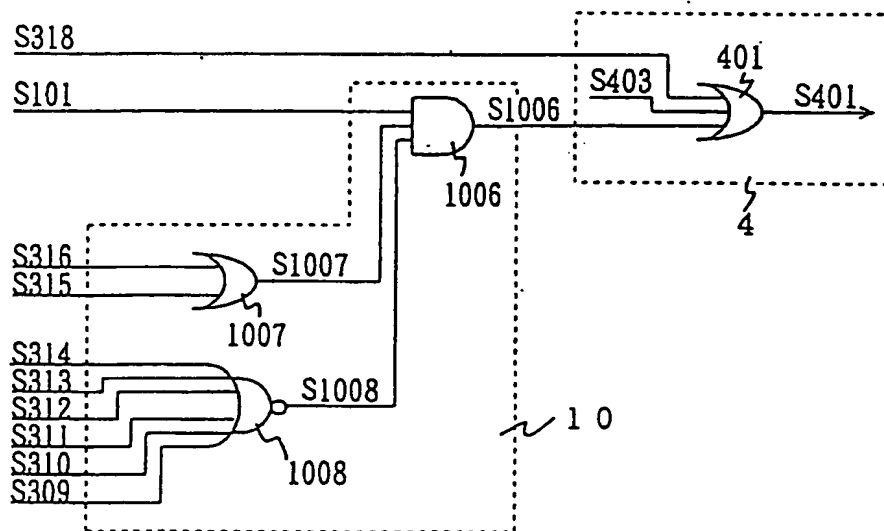


FIG. 42

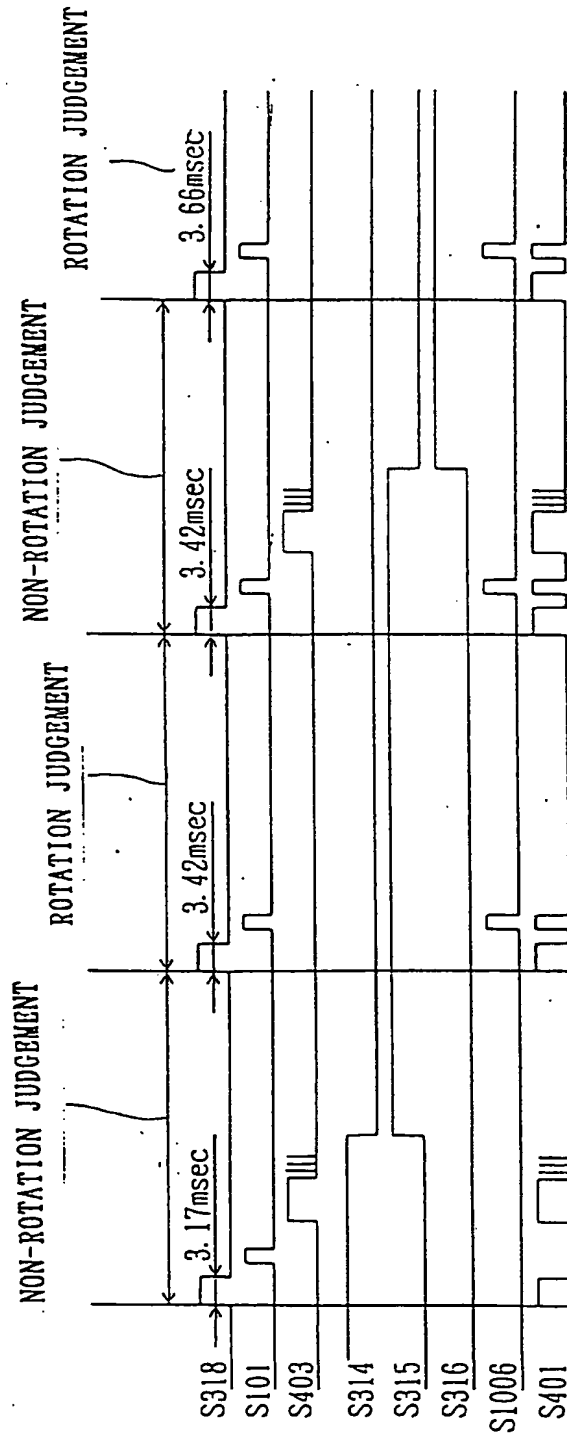


FIG. 43

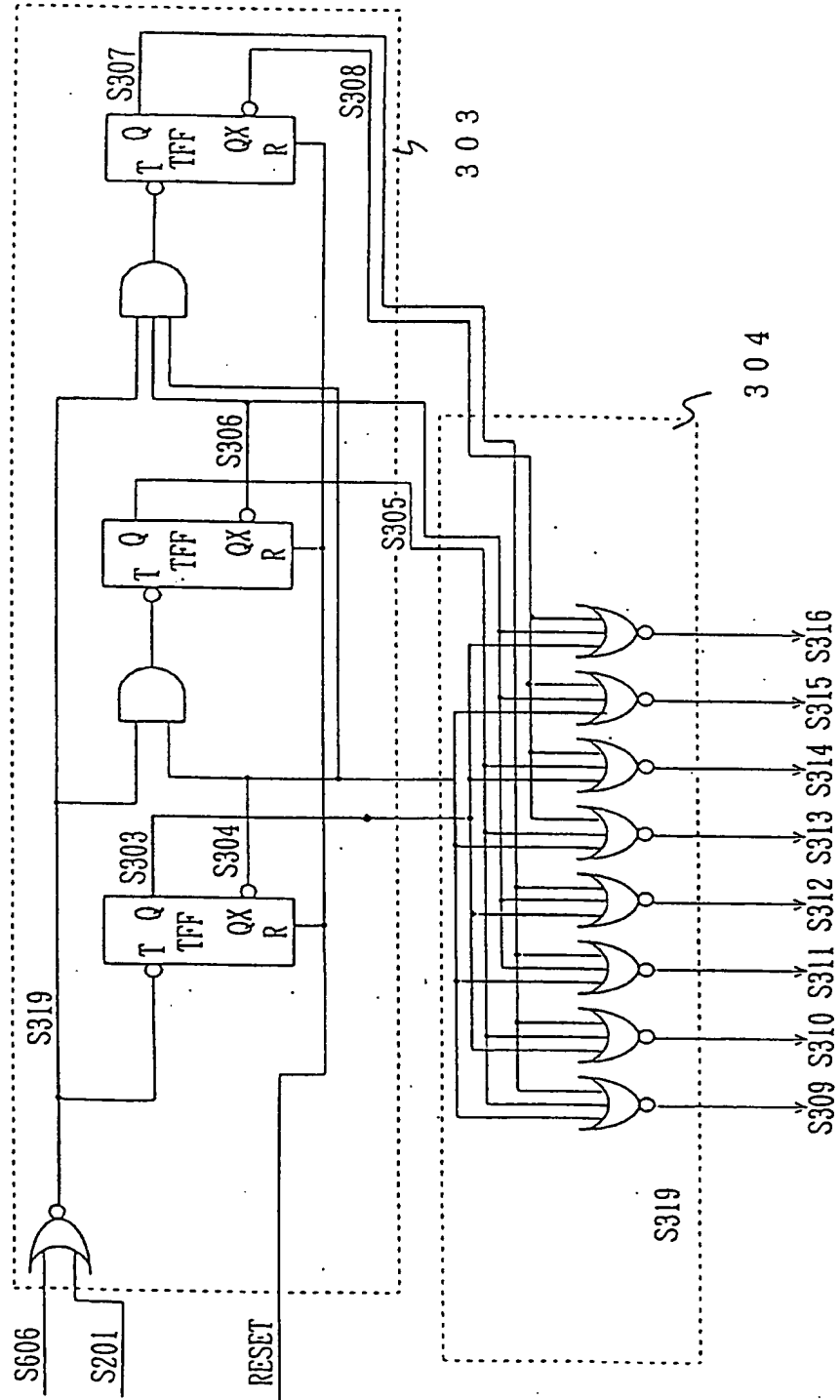


FIG. 44

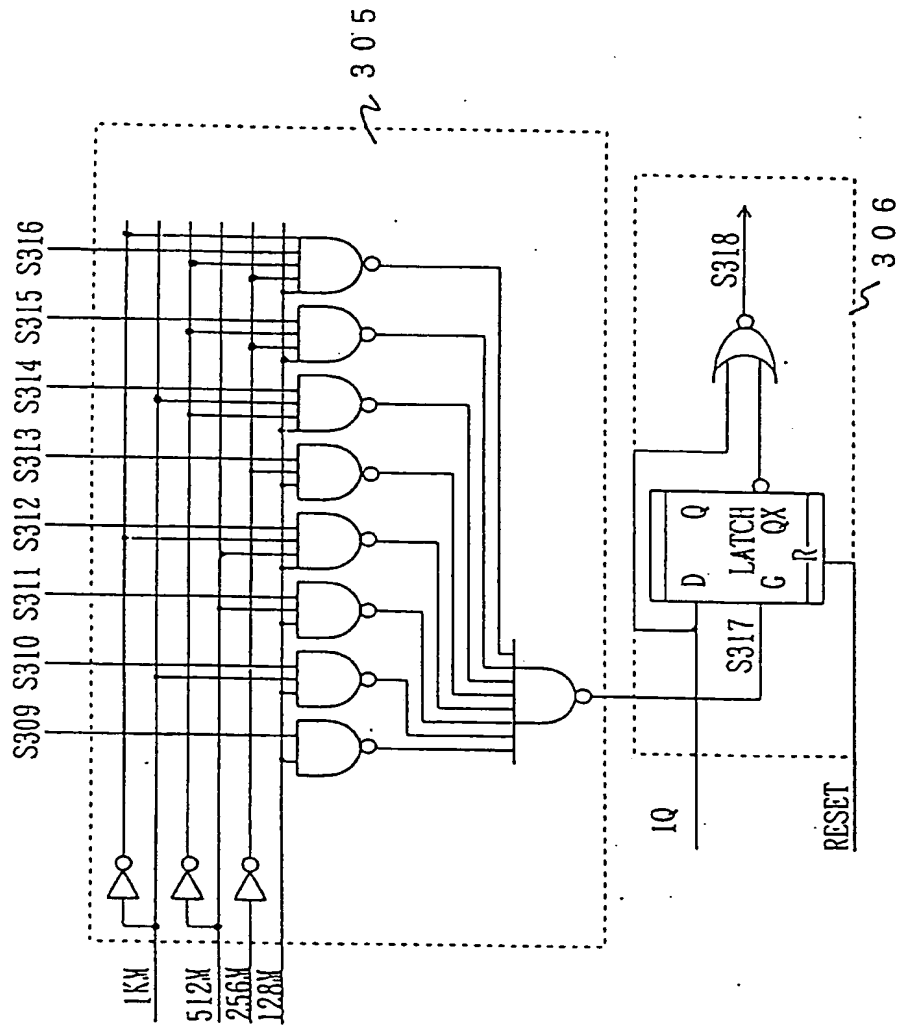


FIG. 45

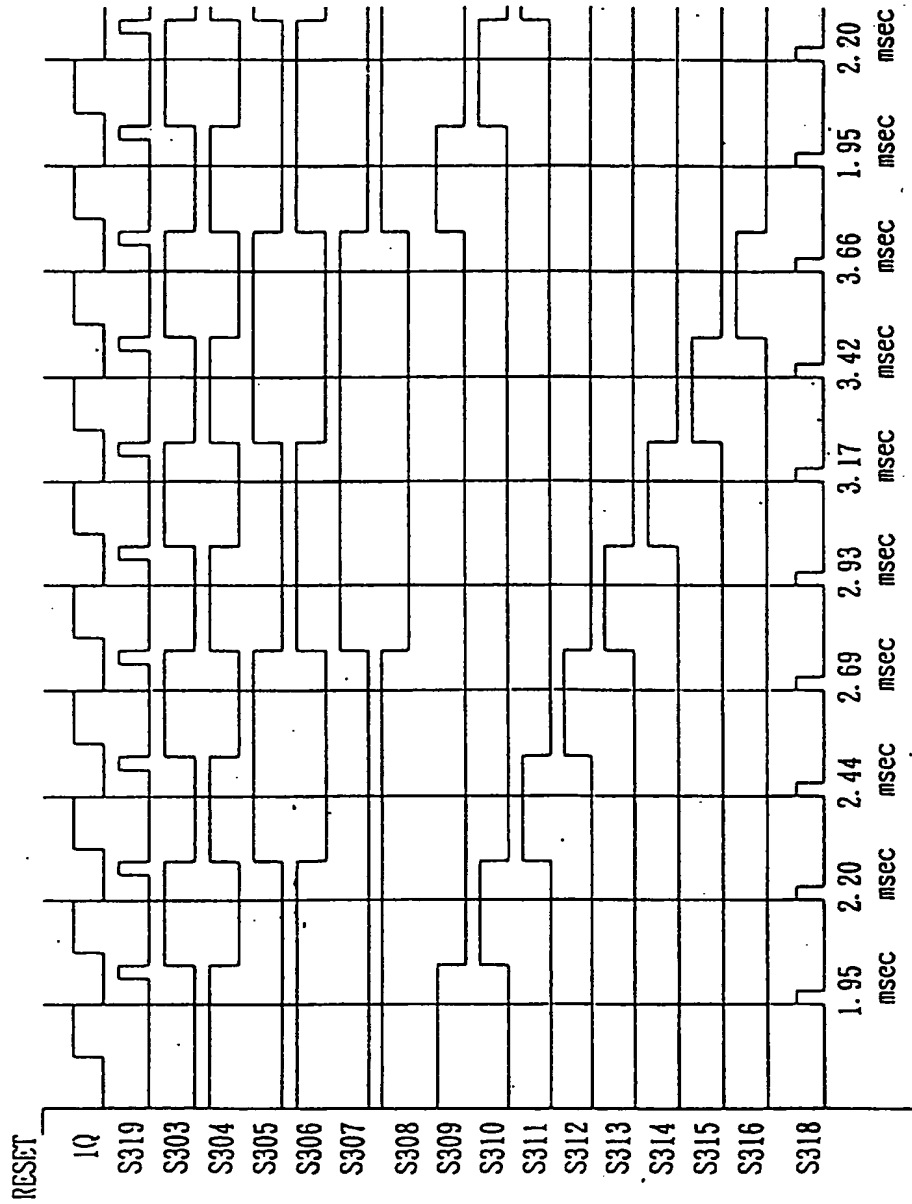


FIG. 46

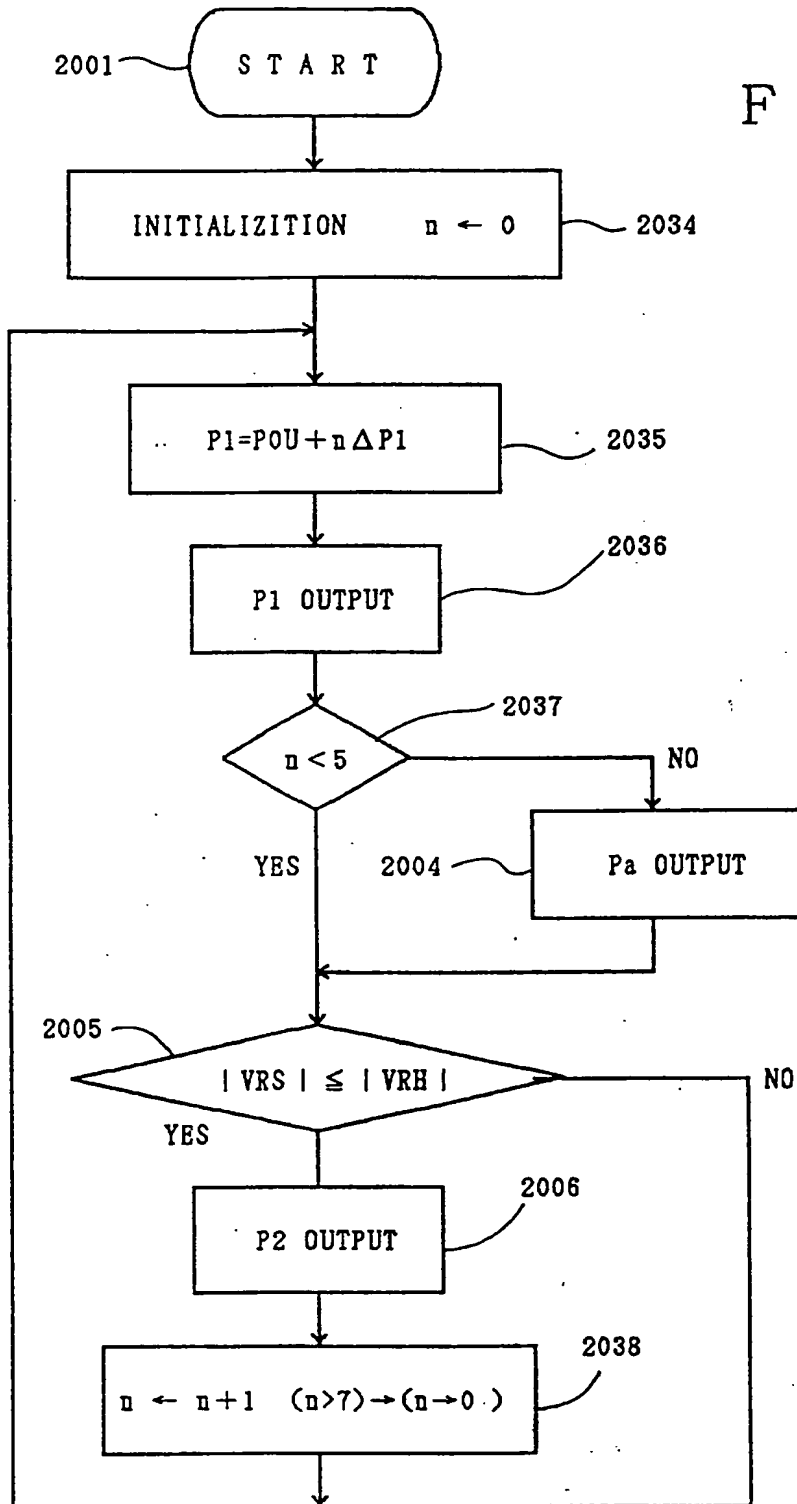


FIG. 47

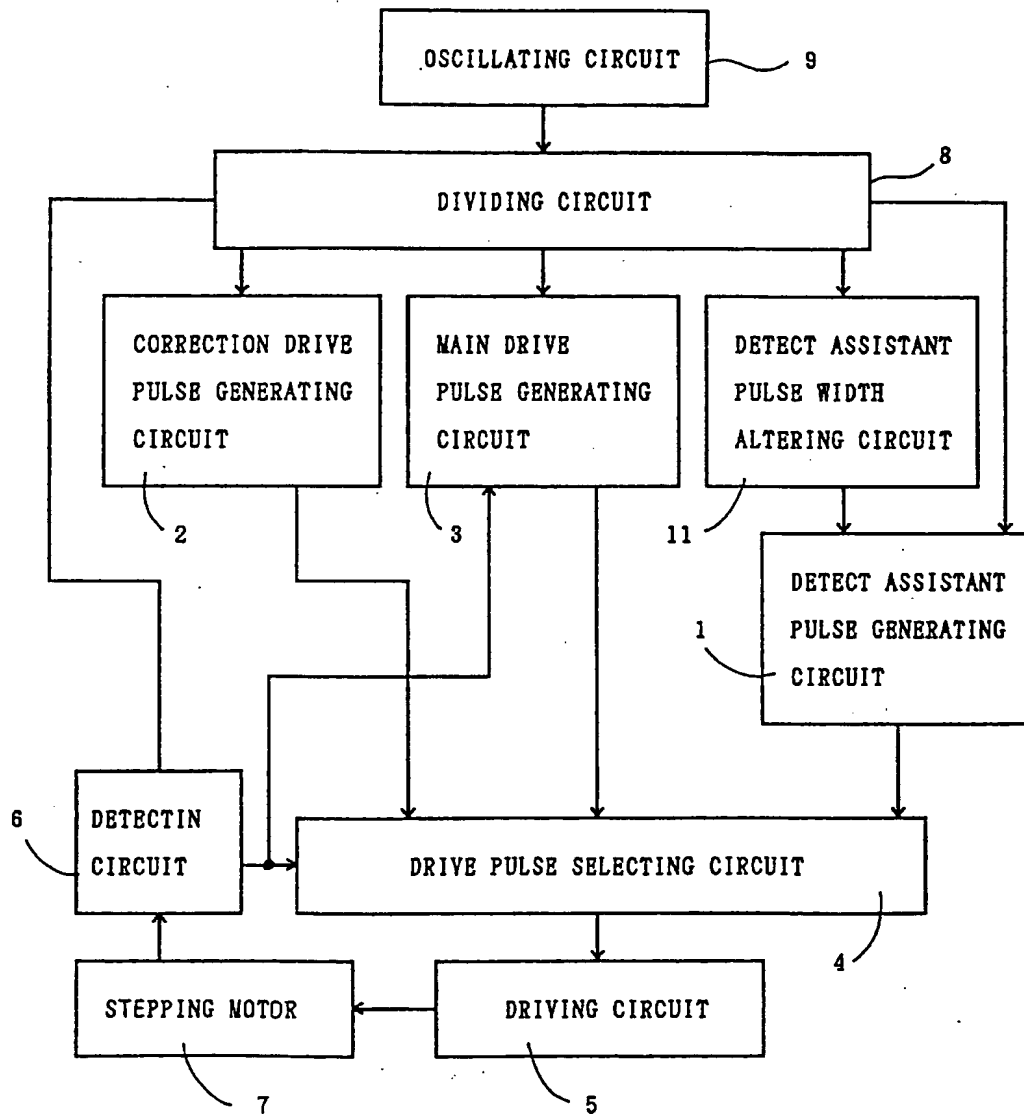


FIG. 48

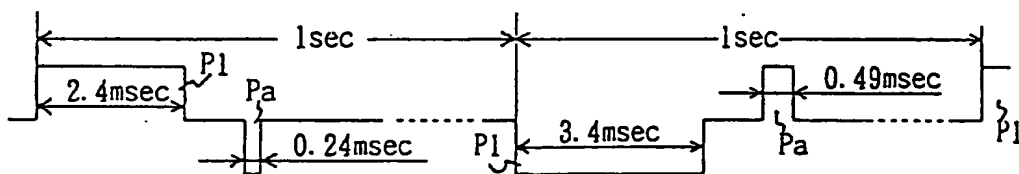
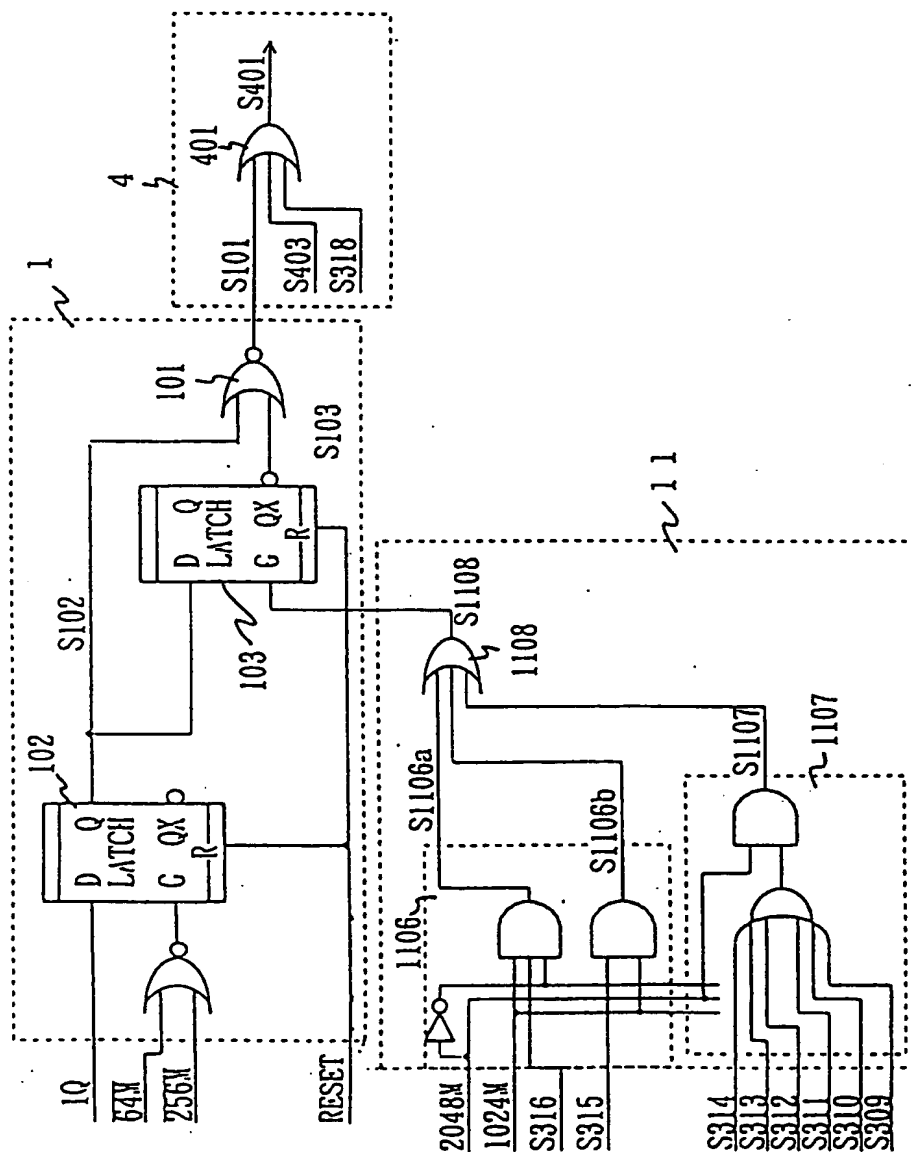


FIG. 49



Timing diagram for the S316 instruction. The diagram shows the relationship between the instruction bus (IQ) and the data bus (SI) for the S316 instruction. The instruction bus (IQ) is high for 4.80msec. The data bus (SI) is high for 0.36msec. The instruction bus (IQ) is high for 0.24msec. The data bus (SI) is high for 0.12msec. The diagram is divided into three sections: "S316 is High", "S315 is High", and "S309 ~ S314 is High".

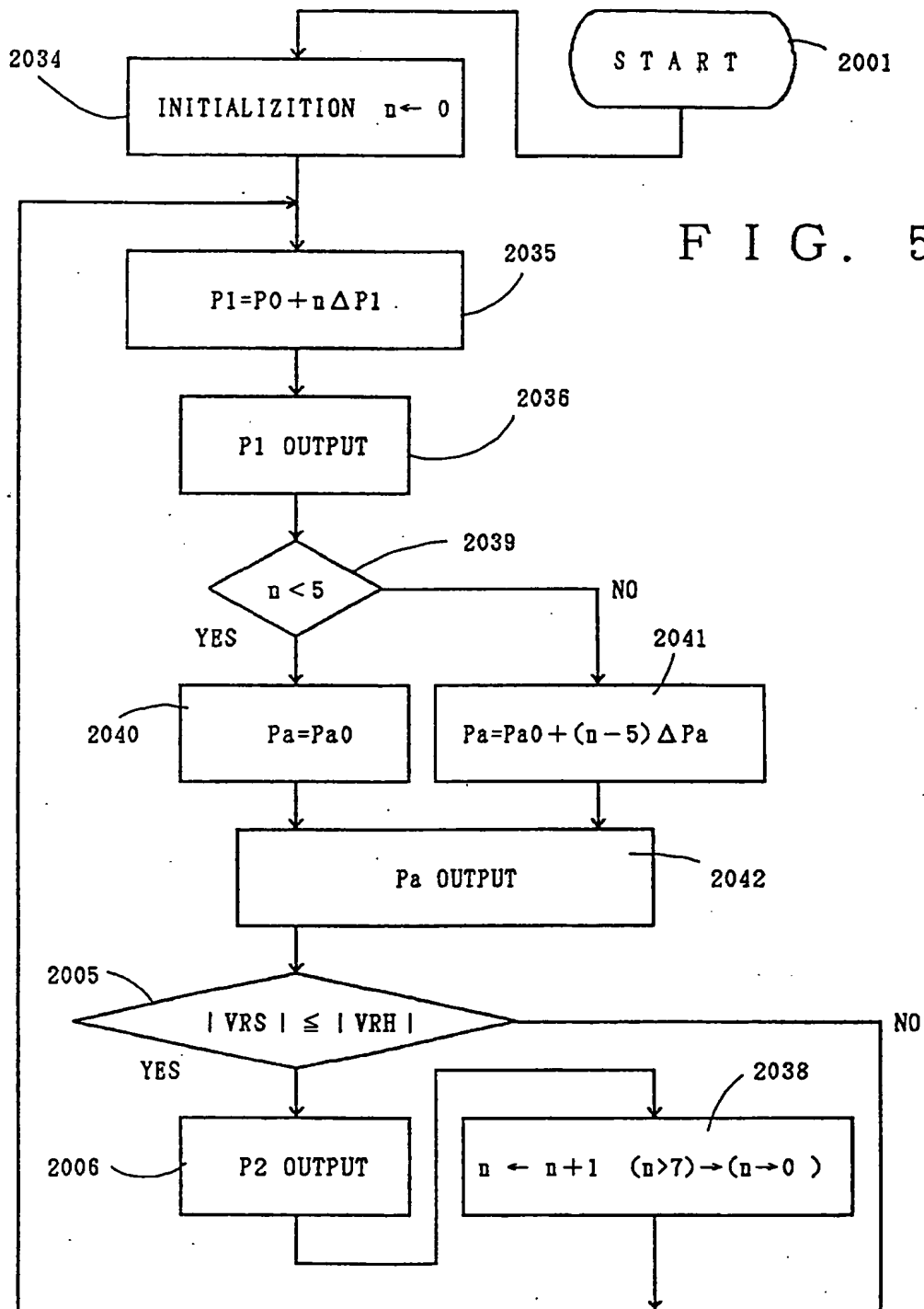


FIG. 52

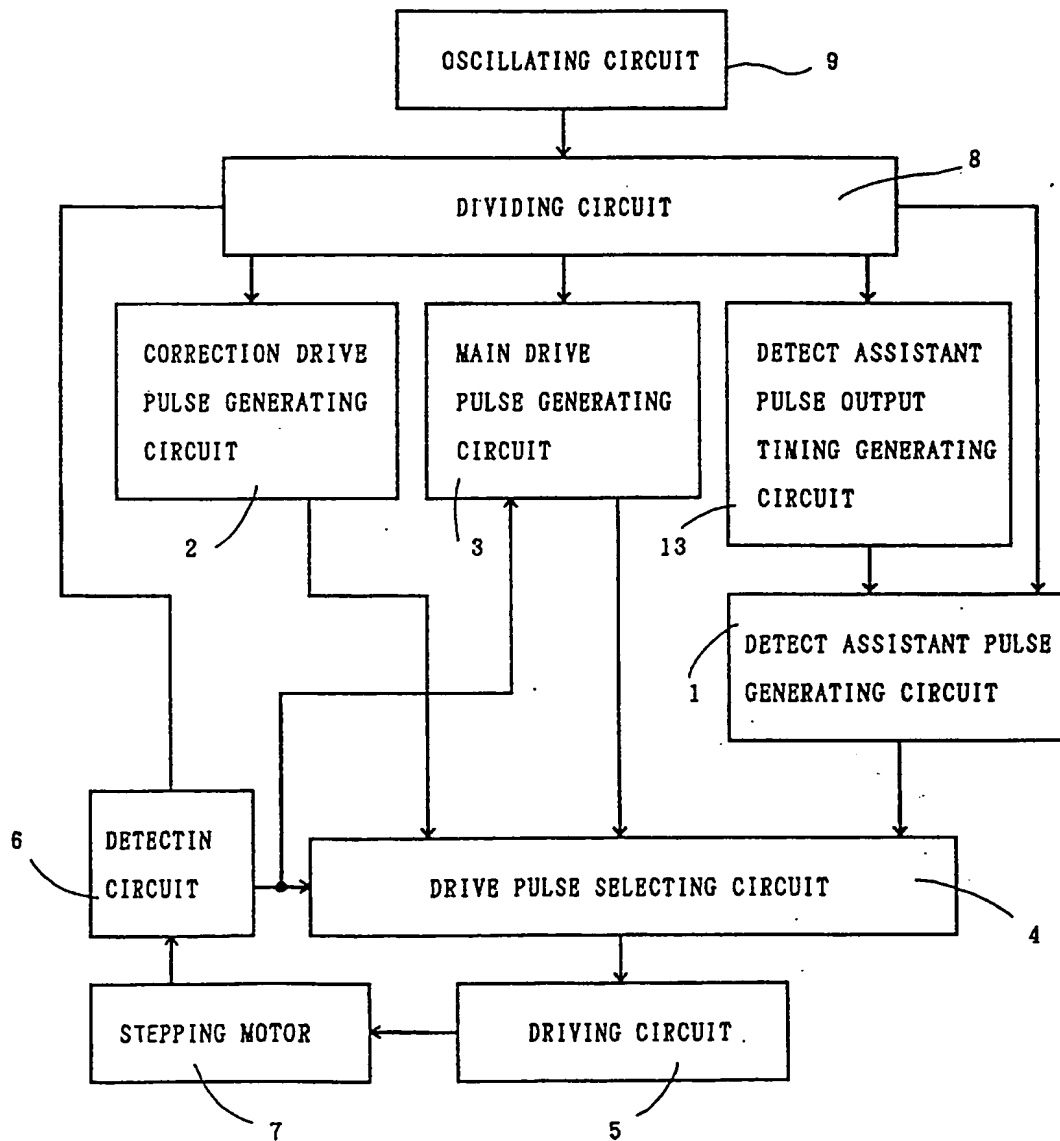


FIG. 53

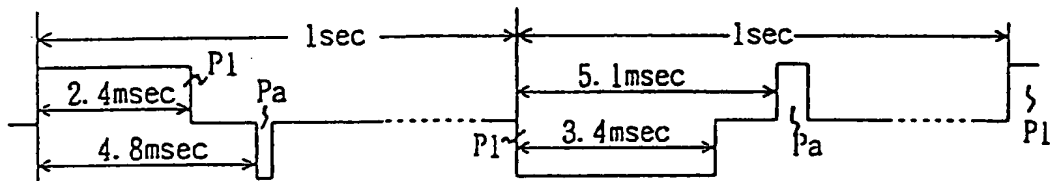


FIG. 54

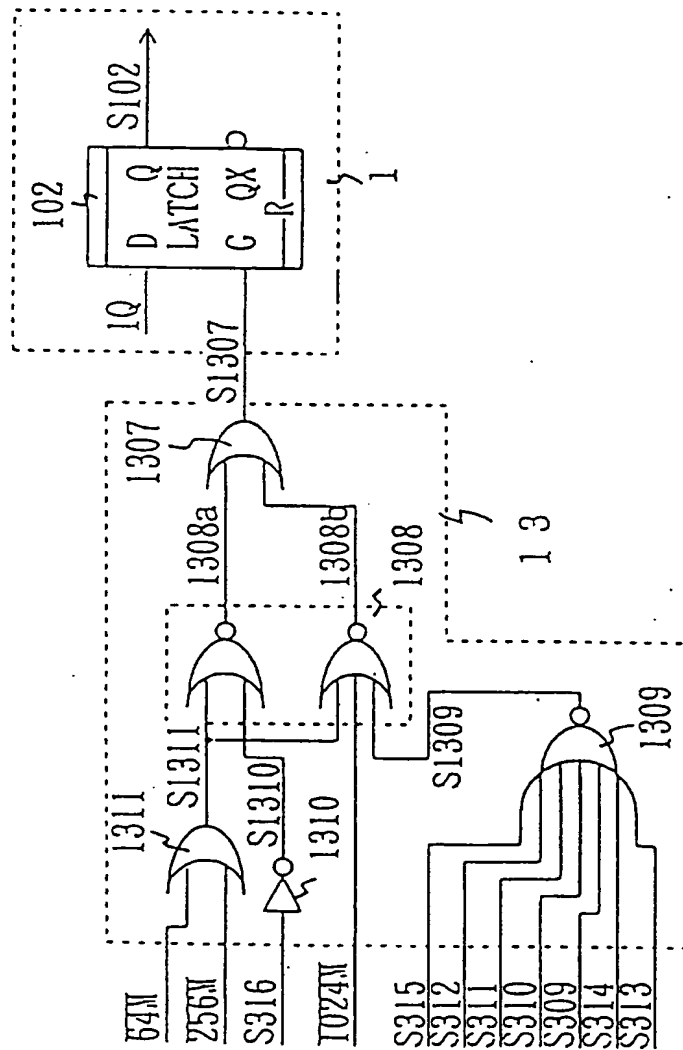
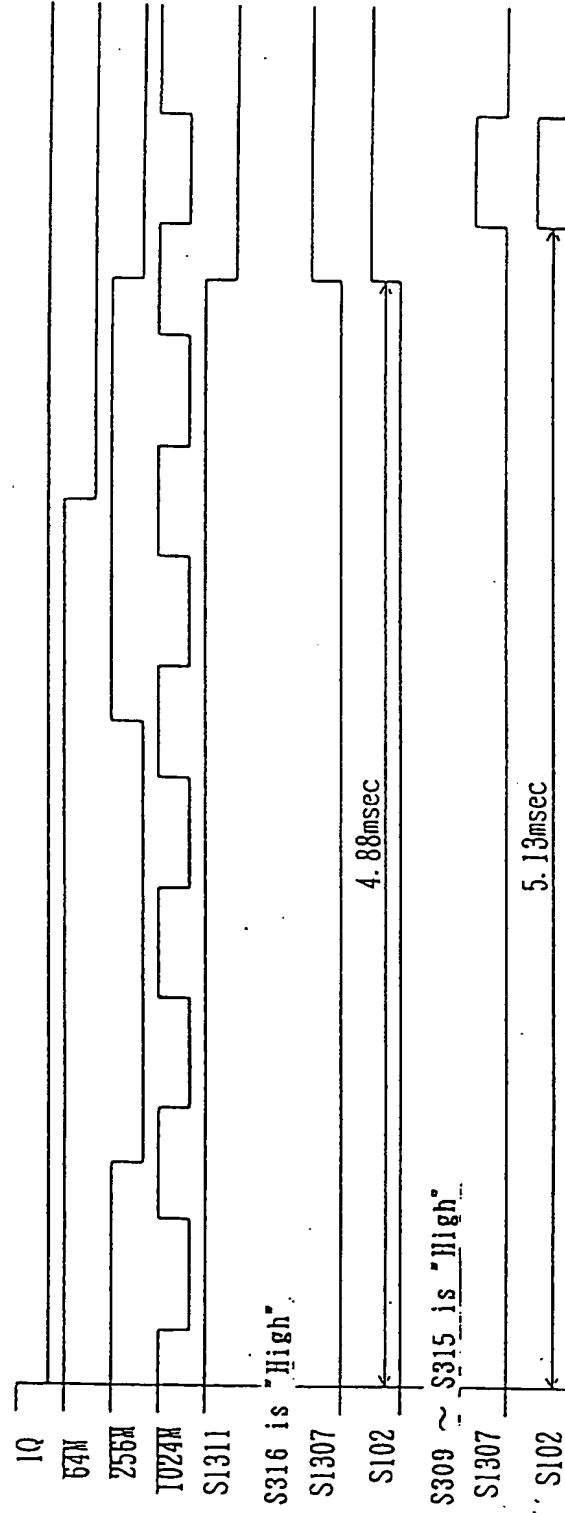


FIG. 55



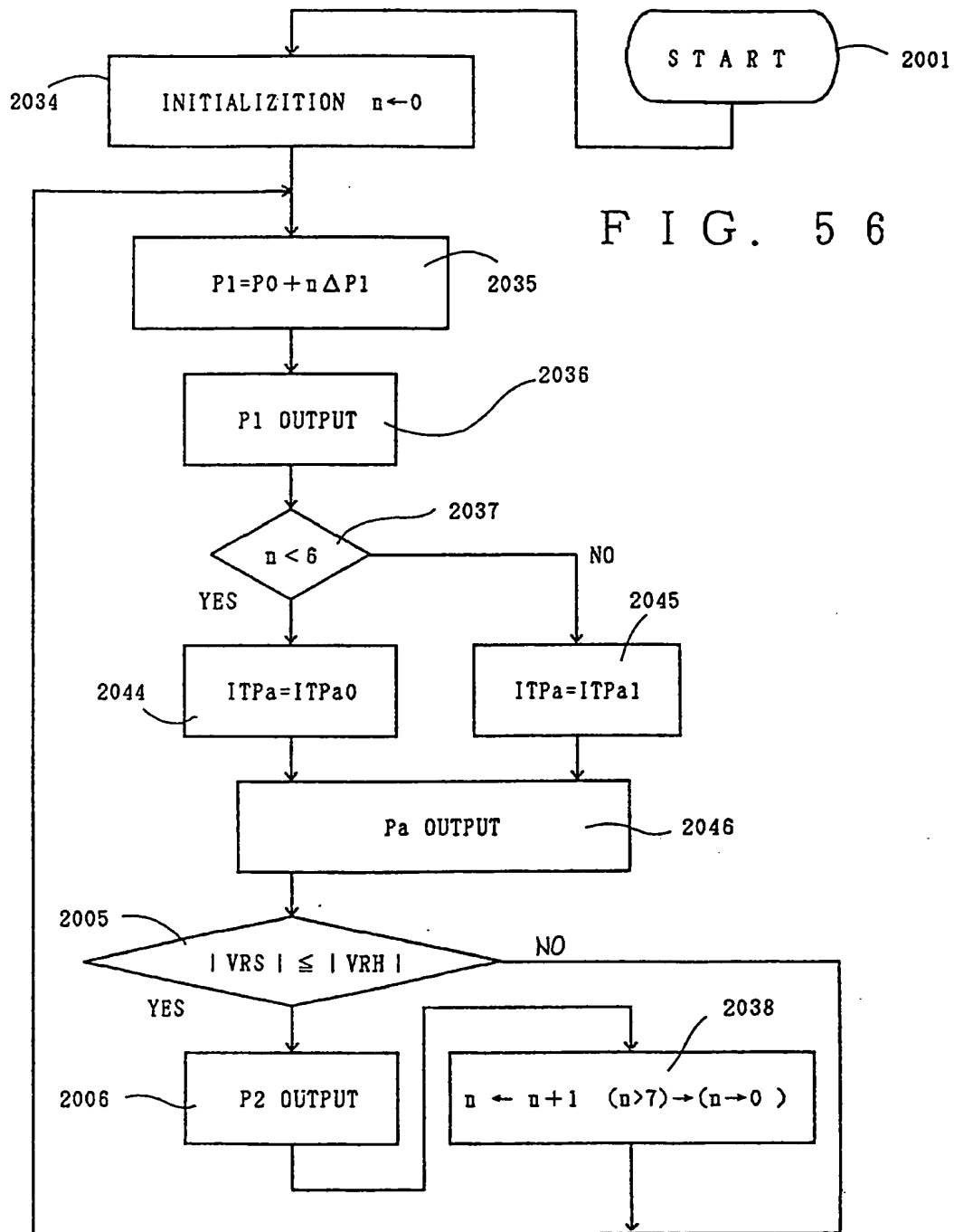
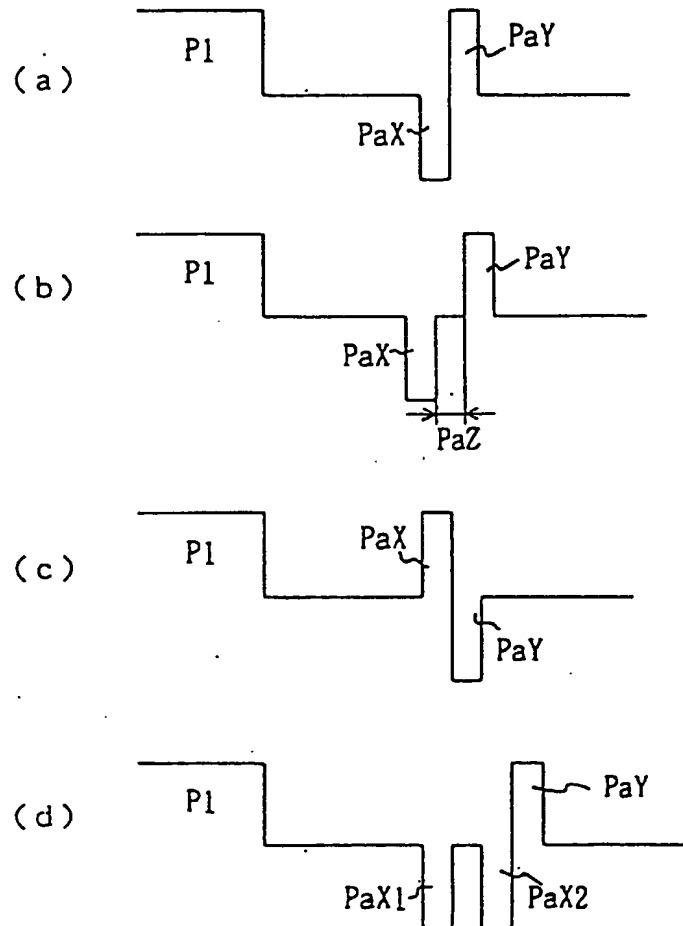


FIG. 57



INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP94/00030

A. CLASSIFICATION OF SUBJECT MATTER		
Int. Cl ⁵ G04C3/14		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
Int. Cl ⁵ G04C3/14		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Jitsuyo Shinan Koho 1926 - 1993		
Kokai jitsuyo Shinan Koho 1971 - 1993		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, B2, 3-26355 (Seiko Epson Corp.), April 10, 1991 (10. 04. 91) & US, A, 4477196 & GB, B2, 2101368 & CH, B, 648179 & DE, C2, 3217207 & HK, A, 73986 & SG, A, 53386	1
Y	Columns 3 to 4, Fig. 3	2-9
A	Figs. 3 to 11	3-9
A	JP, B2, 61-28317 (Seiko Instruments Inc.), June 30, 1986 (30. 06. 86), Fig. 11, (Family: none)	4, 7
A	JP, A, 58-66089 (Seikosha Co., Ltd.), April 20, 1983 (20. 04. 83), Fig. 2, (Family: none)	5, 8
A	JP, U, 2-22098 (Seiko Epson Corp.), December 14, 1990 (14. 02. 90), Figs. 1 to 3, (Family: none)	
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier document but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reasons (as specified) "O" document referring to as oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
February 25, 1994 (25. 02. 94)		March 15, 1994 (15. 03. 94)
Name and mailing address of the ISA/ Japanese Patent Office		Authorized officer
Facsimile No.		Telephone No.